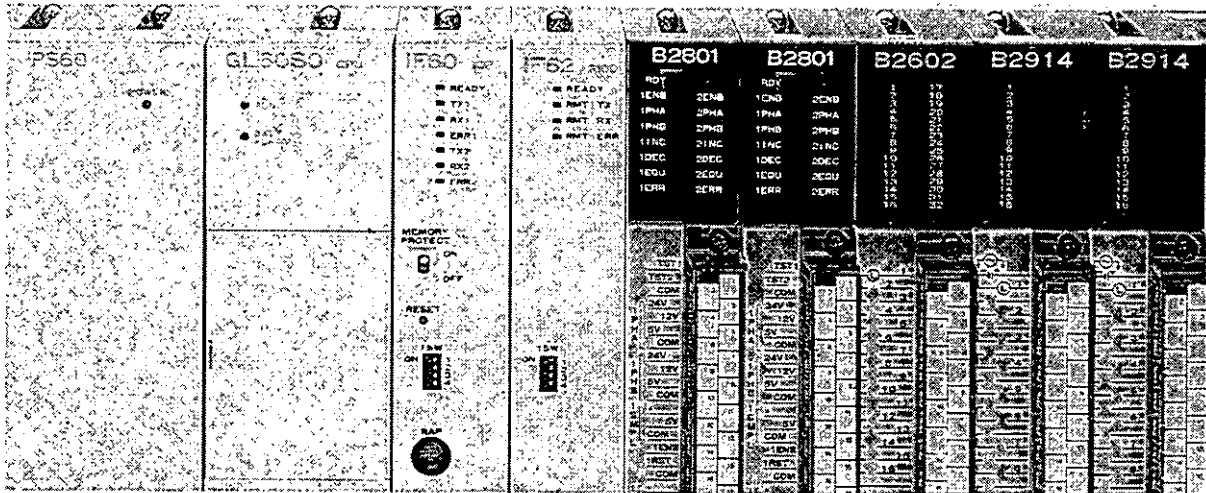


MEMOCON-SC 2000 SERIES I/O REVERSIBLE COUNTER MODULE B2801 DESCRIPTIVE INFORMATION

MEMOCON-SC GL40S, GL60S, GL60H, GL70H



NOTES FOR SAFE OPERATION


Read these manuals thoroughly before use of Reversible Counter Module B2801. In this manual, NOTES FOR SAFE OPERATION are classified as “WARNING” and “CAUTION.”



: Indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury to personnel.



: Indicates a potentially hazardous situation which, if not avoided, may result in minor or moderate injury to personnel and damage to equipment. It may also be used to alert against unsafe practices.

Even items described in  CAUTION may result in a vital accident in some situations. In either case, follow these important notes.

The following shows the symbols of prohibition and mandatory action.



: Specifies prohibited handling.



: Specifies actions that must be taken.

After reading these manuals, keep them readily available for those using the equipment.

1 INSTALLATION



CAUTION

- The installation environment must meet the environmental conditions given in the product catalog and manuals.

Using the B2801 in environments subject to high temperatures, high humidity, excessive dust, corrosive gases, vibration, or shock can lead to electric shock, fire, or faulty operation.

— Do not use the MEMOCON-SC in the following locations. —

- Locations subject to direct sunlight or ambient temperatures not between 0 and 55°C.
- Locations subject to relative humidity in excess of 95%, rapid changes in humidity, or condensation.
- Locations subject to corrosive or flammable gas.
- Locations that would subject the MEMOCON-SC to direct vibration or shock.
- Locations subject to contact with water, oil chemicals, etc.

- Do not remove the cover of the connector where a module is not mounted. Foreign matter can cause malfunction in the MEMOCON-SC.
- All screws for installation should be securely tightened and checked for loosening. Malfunctions in the MEMOCON-SC may occur as a result of loose screws.

2 WIRING



CAUTION

- Connect a power supply complying with the rated specifications.
A power supply that does not comply with the rating may cause a fire.
- Wiring must be performed by qualified personnel.
Mistakes in wiring can cause fires, product failure, or malfunctions.
- When wiring, do not allow foreign matters such as wire chip to enter the mounting base or the module.
Foreign matter can cause fires, product failure, or malfunctions.



MANDATORY ACTION

- Ground the protective ground terminal to a resistance of 100Ω max.
Failure to observe this instruction may result in electric shock or malfunction.

NOISE REDUCTION MEASURES

- When noise from external power supply lines causes problems, install an insulated transformer and noise filter for effective noise prevention.
Insufficient noise reduction measure may cause malfunctions in the B2801.



SEPARATE WIRING PROPERLY

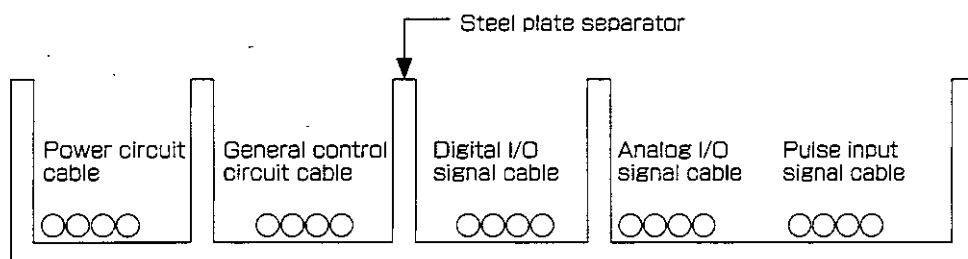
- I/O lines connecting external devices to the B2801 must be selected based on the following considerations :

Mechanical strength, resistance to noise, wiring distance, signal voltage, etc.

- I/O lines must be separated from power lines both within and outside of the control panel to minimize the affects of noise.

Faulty operation can result if I/O lines are not sufficiently separated from power lines.

(Example of external wiring)



3 PRECAUTION UPON USE

⚠ WARNING

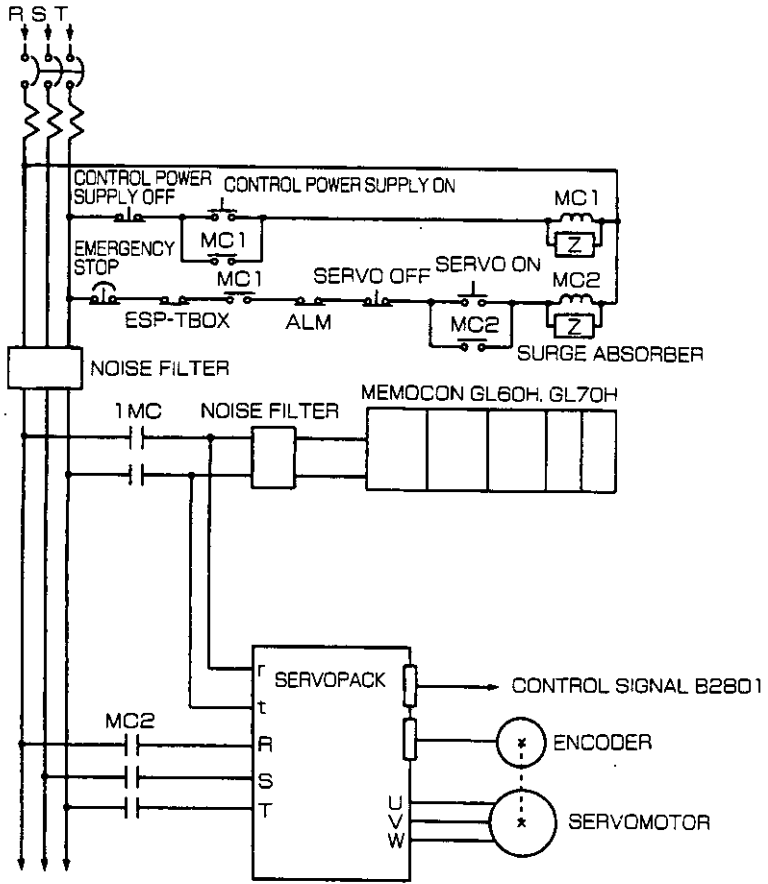
- Do not touch module terminals under current conditions.
There is danger of electric shock.
- Provide an emergency stop circuit, interlock circuit, etc. at the exterior of B2801.
Failure to observe this instruction may result in injury or damage to equipment.

Provide an emergency stop circuit at the exterior of B2801.

An emergency stop circuit for the control system should not be constructed using the ladder programming in the MEMOCON-SC. Install an emergency stop circuit to an external relay as shown below.

Use a NC contact (mechanical contact) to connect the emergency stop switch. The emergency stop switch should cut off the main power supply when depressed.

If these steps are not followed, the emergency switch will not engage even if input circuits are damaged or cables are cut. Failure to follow instructions may cause damage to machines and injury to personnel.



4 MAINTENANCE

PROHIBITION

- Do not attempt to disassemble or modify the MEMOCON-SC in any way. Doing so can cause fires, product failure, or malfunctions.

CAUTION

- Attaching, installing or removing other Modules is only to be made after the power is turned OFF. Otherwise, electric shock, malfunction or breakdown will result.

5 GENERAL PRECAUTION

- MEMOCON-SC was not designed or manufactured for use in devices or systems that concern peoples' lives. Users who intend to use the product described in this manual for special purposes such as devices or systems relating to transportation, medical, space aviation, atomic power control, or underwater use must contact YASKAWA representatives beforehand.
- This product has been manufactured under strict quality control guidelines. However, if this product is to be installed in any location in which a failure of MEMOCON-SC involves a life and death situation or in a facility where failure may cause a serious accident, safety devices must be installed to minimize the likelihood of any accident.
- Any illustrations, photographs, or examples used in this manual are provided as examples only and may not apply to all product to which this manual is applicable.
- The products and specifications described in this manual or the content and presentation of the manual may be changed without notice to improve the product and/or the manual. A new version of the manual will be re-released under a revised document number when any changes are made.
- Contact your YASKAWA representative listed on the back of this manual to order a new manual whenever this manual is damaged or lost. Please provide the document number listed on the front cover of this manual when ordering.
- Contact your YASKAWA representative listed on the back of this manual to order new nameplates whenever a nameplate becomes worn or damaged.
- YASKAWA cannot make any guarantee for products which have been modified. YASKAWA assumes no responsibility for any injury or damage caused by a modified product.

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1. OVERVIEW OF MANUAL

- This manual describes functions, specifications, and application methods of the MEMOCON-SC GL40S, GL60S, GL60H, GL70H 2000 Series Reversible Counter Module B2801.
- Read this manual carefully in order to use the Reversible Counter Module properly. Also, keep it in a safe place so that it can be used whenever necessary.
- Refer to the following manuals as necessary.

	Document Title	Document Number	Content
CPU Module	MEMOCON-SC GL60S DESCRIPTIVE INFORMATION	SIE-C815-14.1	Describes system configuration devices and their functions, specifications, application methods, etc., for the MEMOCON-SC GL60S.
	MEMOCON-SC GL40S DESCRIPTIVE INFORMATION	SIE-C815-15.1	Describes system configuration devices and their functions, specifications, application methods, etc., for the MEMOCON-SC GL40S.
	MEMOCON-SC GL60H/GL70H DESCRIPTIVE INFORMATION	SIE-C815-17.1	Describes system configuration devices and their functions, specifications, application methods, etc., for the MEMOCON-SC GL60H/GL70H.
Man/ Machine Interface	MEMOCON-SC GL60S P150 PROGRAMMING PANEL DESCRIPTIVE INFORMATION	SIE-C815-14.2	Describes functions, specifications, application methods, etc., for the P150 PROGRAMMING PANEL.
	MEMOCON-SC GL60S P150 PROGRAMMING PANEL DESCRIPTIVE INFORMATION	SIE-C815-14.3	Describes the SFC functions, specifications, application methods, etc., for the P150 Programming Panel.
I/O Module	MEMOCON-SC GL40S, GL60S GL70H 2000 SERIES I/O MODULES DESCRIPTIVE INFORMATION	SIE-C815-13.3	Describes functions, specifications, application methods, etc., for the 2000 Series Digital I/O Modules.

*Thoroughly check the specification and conditions of the product before use.

USING THIS MANUAL

This manual is written for those who already have basic knowledge of MEMOCON-SC. We recommend reading the MEMOCON-SC GL40S, GL60S and GL60H, GL70H Descriptive Information before reading this manual.

• Meaning of Basic Terms

In this manual, the following terms indicate the meanings as described below, unless otherwise specified.

- B2801 = 2000 Series Reversible Counter Module JAMSC-B2801
- PC = Programmable Controller
- PP = Programming Panel
- GL40S, GL60S, GL60H, GL70H = MEMOCON-SC GL40S, GL60S, GL60H, GL70H Programmable Controllers

2. CONFIGURATION

An example of B2801 system configuration is shown in Fig. 2. 1 (using GL20 for CPU and two B2801 units.)

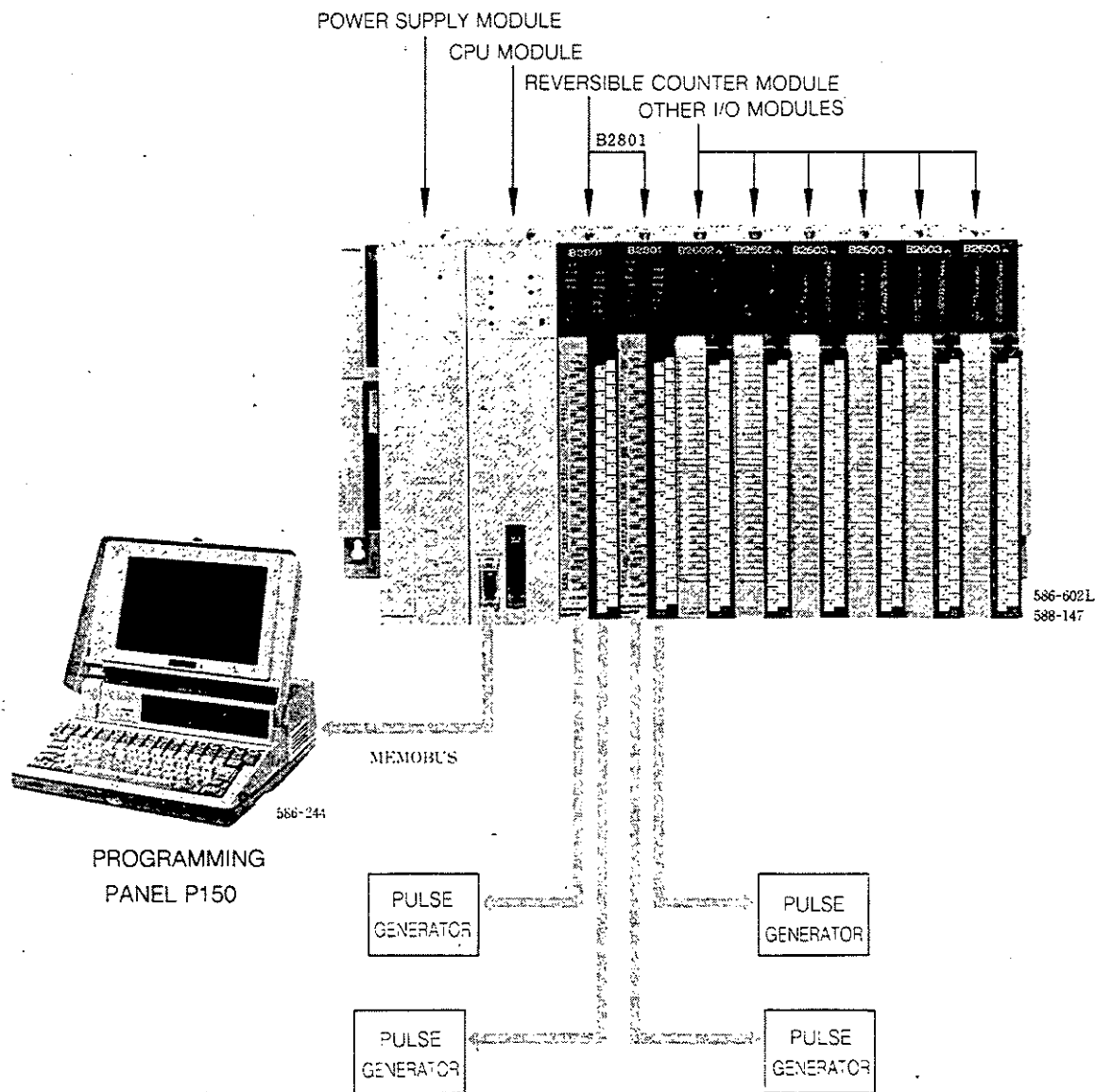


Fig. 2. 1 B2801 System Configuration

3. SPECIFICATIONS

3.1 GENERAL SPECIFICATIONS

Table 3.1 General Specifications

Item	Specification
Model	JAMSC-B2801
Ambient Temperature	0 to + 55°C
Storage Temperature	-20 to + 85°C
Humidity	10 to 90% RH (non-condensing)
Vibration Resistance	In compliance with JIS* C0911 (Range: 10 to 55 Hz, amplitude: 0.075mm, No. of liftings: 10 times)
Shock Resistance	In compliance with JIS* C0912 (10G max.)
Environmental Condition	Free from explosive, inflammable and/or corrosive gases.
Dielectric Strength, Resistance	Strength: 1500 VAC for one minute (Internal circuit against external circuit) Resistance: 500VDC, 100MΩ min.
Noise Resistance	1500V, 1μs, 1ns, at startup, by noise simulator
Dimensions in mm (inches)	38(1.50)W × 250(9.84)H × 104(4.10)D †, 1 span
Weight	Approximately 0.6kg
Internal Consumable Current (Vcc)	5VDC ± 3% 0.25A

*Japanese Industrial Standard

† Including terminal block

3. 2 PERFORMANCE SPECIFICATIONS

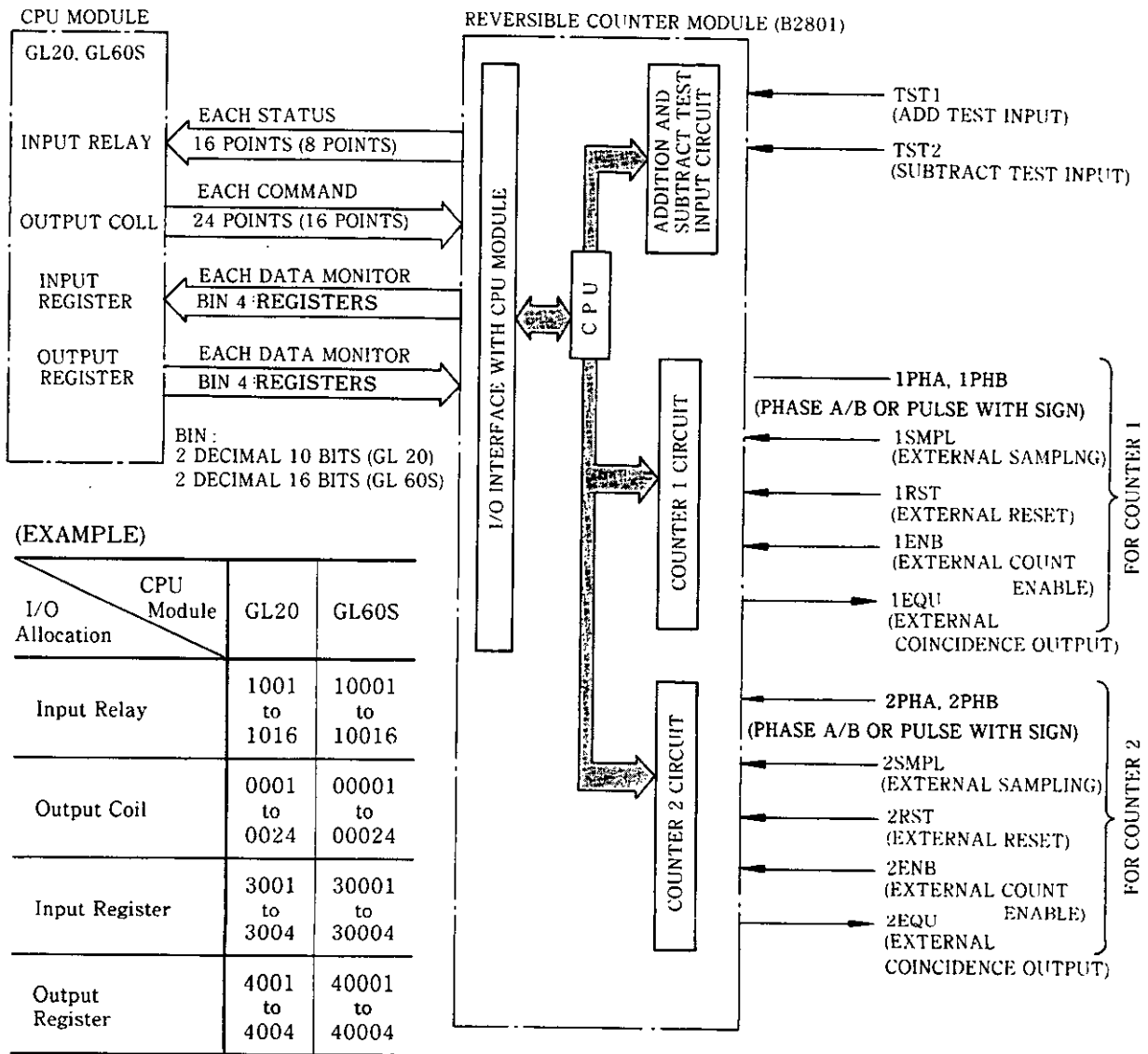
Table 3. 2 Performance Specifications

Item	Specification	Remarks	
Function	Pulse count and output of external coincidence signal	—	
Number of Counter Circuits	Two independent circuits	—	
Adaptable CPU Module	GL20, GL60	Selected by a switch	
I/O Allocation, Points/Sets	Input relay : 16 points (also 8 points) Output coil : 24 points (also 16 points) Input register : 4 registers binary allocation Output register : 4 registers binary allocation	Number of allocations for CPU modules	
Count Specification	Counter Digits	6-digit decimal (GL20) . 8-digit decimal (GL60S)	Selected by a switch
	Maximum Counting Speed	50kpps (Multiplier 1), 100kpps (Multiplier 2), 20kpps (Multiplier 4)	—
	Counting Pulse Method	Phase A/B (Multipliers 1, 2 and 4), pulse with sign (Multiplier 1)	Selected by initial setting
	Pulse Input Voltage	5VDC, 12V, 24V	Selected by terminal block
Counter Functions	Comparison counter, Sampling counter, Memory counter	Selected by initial setting (combination of counter functions can be freely set by counters 1 and 2.)	
External Test Input	ADD test, SUBTRACT test	Common to counters 1 and 2. Corresponds to 12V and 24V.	
External Input Signal	(External count enable, external reset, external sampling) x1 point/circuit.	Corresponds to 12 V and 24 V inputs.	
External Output Signal	External coincidence output x 1 point/circuit.	Open collector output, requires 12V or 24V power supply.	
Monitor Function	Provided.	—	
External Power Supply	Corresponds to 5/12/24V.	Refer to Par. 6. 2.	

Note : Initial setting means that the B2801 counter functions are initialized by ladder circuits (refer to Par. 5. 4. 1).

3.3 INTERFACE OF CPU MODULE AND EXTERNAL DEVICES

Fig. 3.1 shows the interface of B2801, CPU module (GL20, GL60S) and external devices.



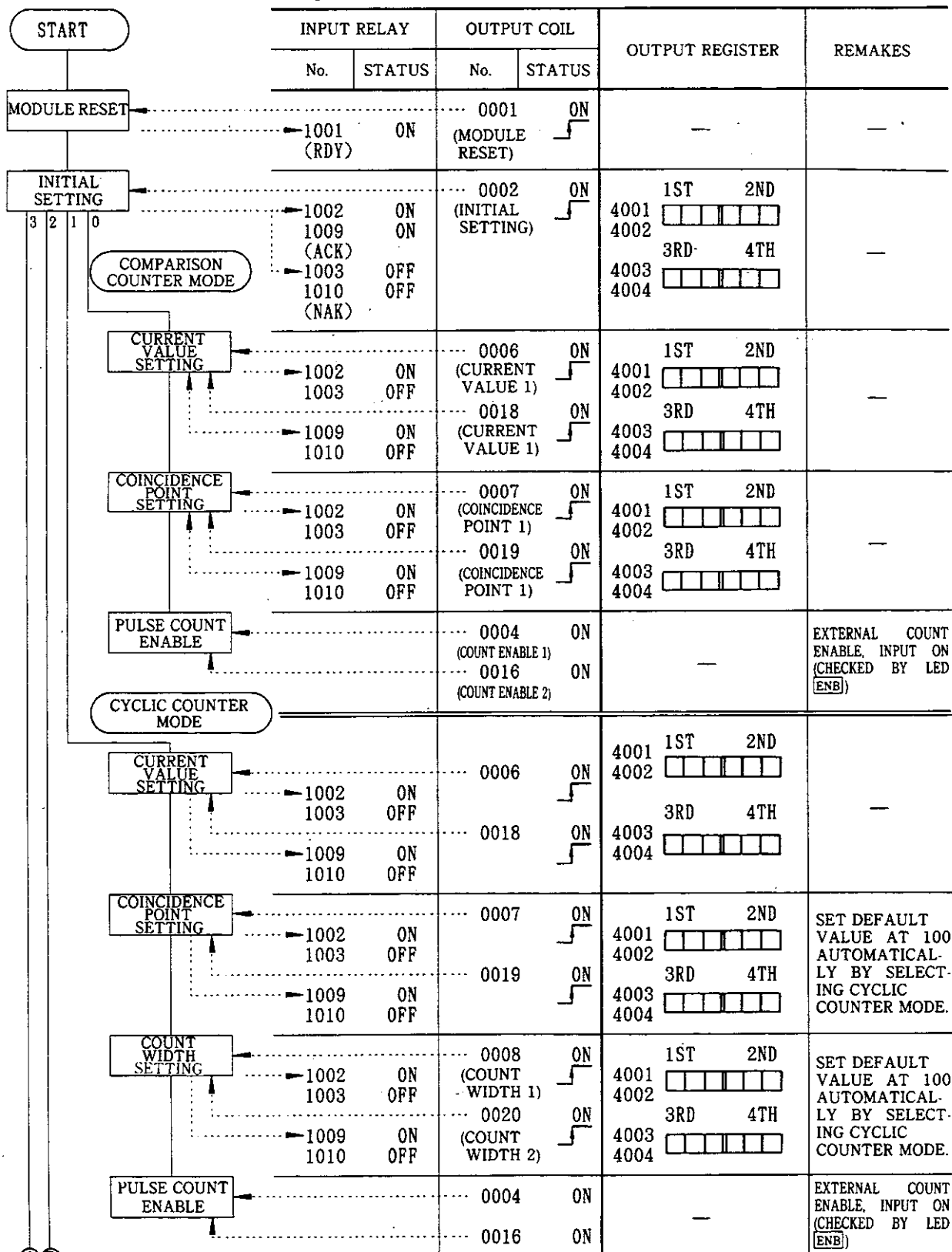
(Refer to Par. 5 INTERNAL INTERFACE.)

Fig. 3.1 Interface of CPU Module and External Devices

3. 4 B2801 OPERATION FLOW

B2801 is provided with counters 1 and 2 which can be set with independent counter functions.
 Fig. 3. 2 shows B2801 operation outline. (The reference numbers here are given as an example.)

Setting and Conditions by CPU Module (GL20) (Refer to Par. 5.)



Note : shows start-up from OFF to ON.

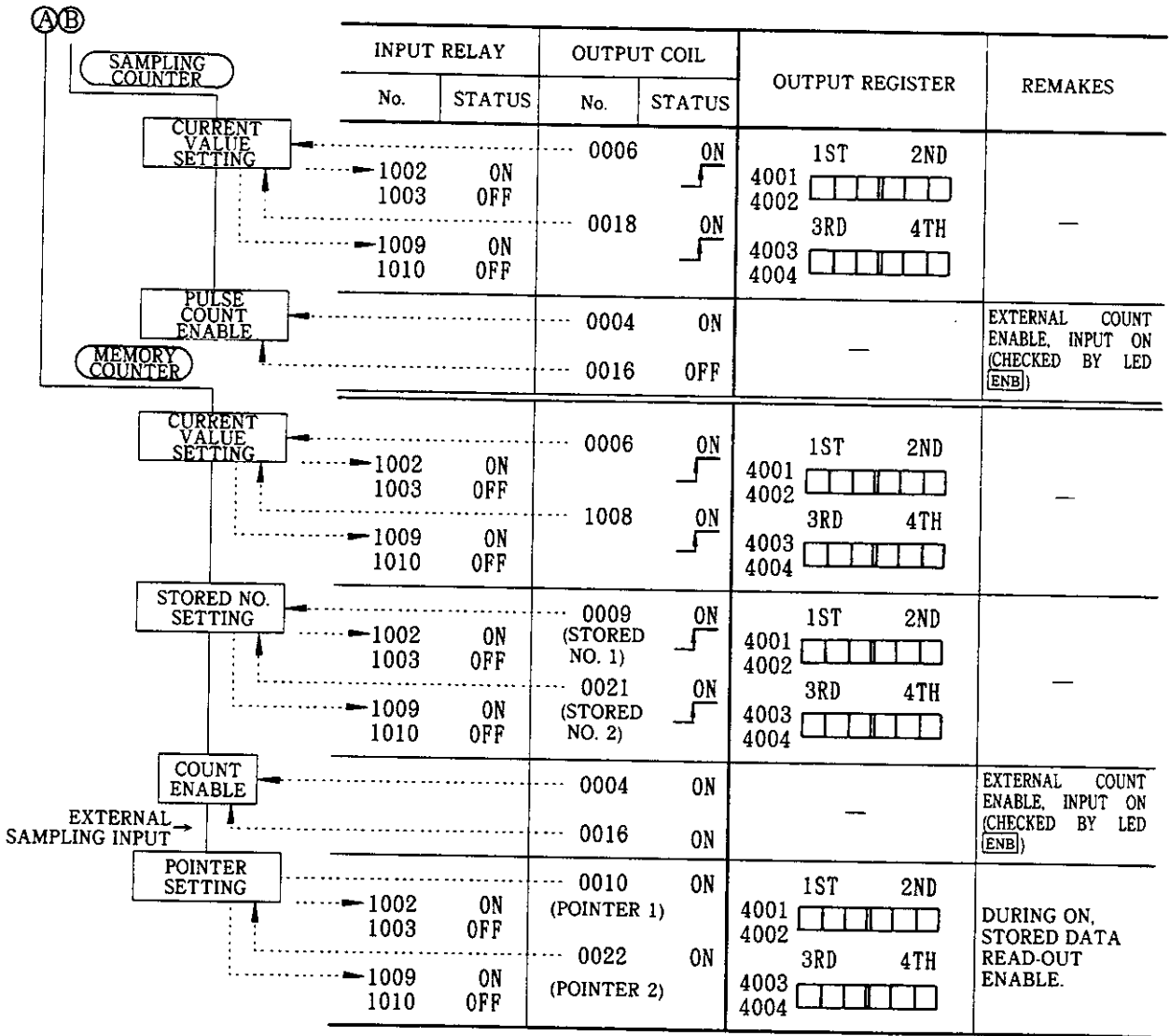


Fig. 3. 2 B2801 Operation Flow

4. COUNTER FUNCTIONS

The B2801 has four counter functions. Comparison counter, cyclic counter, sampling counter and memory counter. They can be specified by the initial setting. Counter functions can be independently set for counters 1 and 2. Each counter function is explained in the following paragraphs. Counter number is shown in which follows a signal name.

NOTE

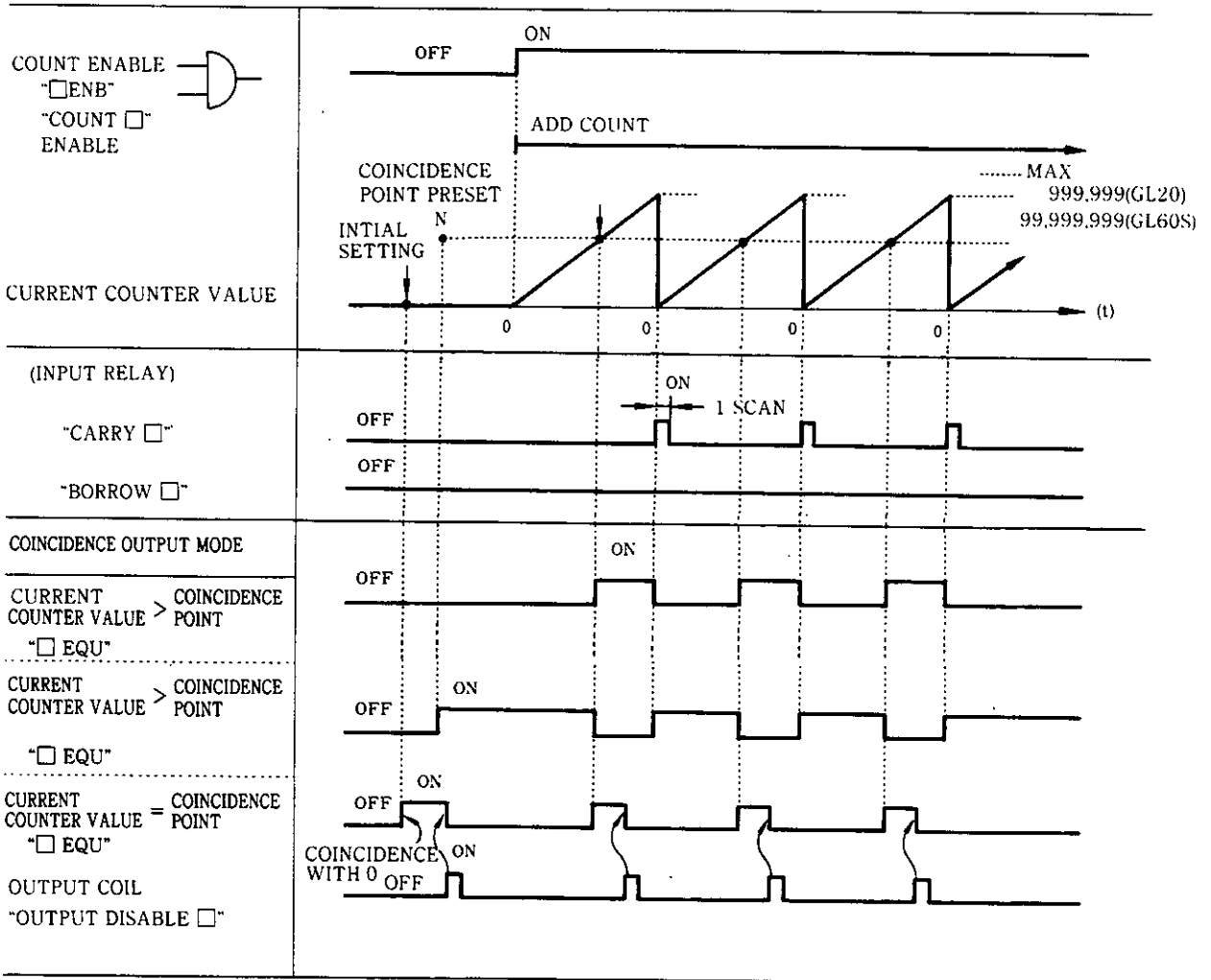
Count operation continues even if CPU is not operating.

4. 1 COMPARISON COUNTER FUNCTION

(1) In addition to pulse count function (with carry and borrow) the comparison counter has an external coincidence output which turns on/off based on comparison between a current counter value and a coincidence setting value from the CPU module.

There are three coincidence output modes ($>$, $=$, $<$) in the comparison. The external coincidence output ON/OFF varies depending on its mode. Coincidence output mode is specified by the initial setting.

Figs. 4. 1 and 4. 2 show basic operation of the comparison counter.

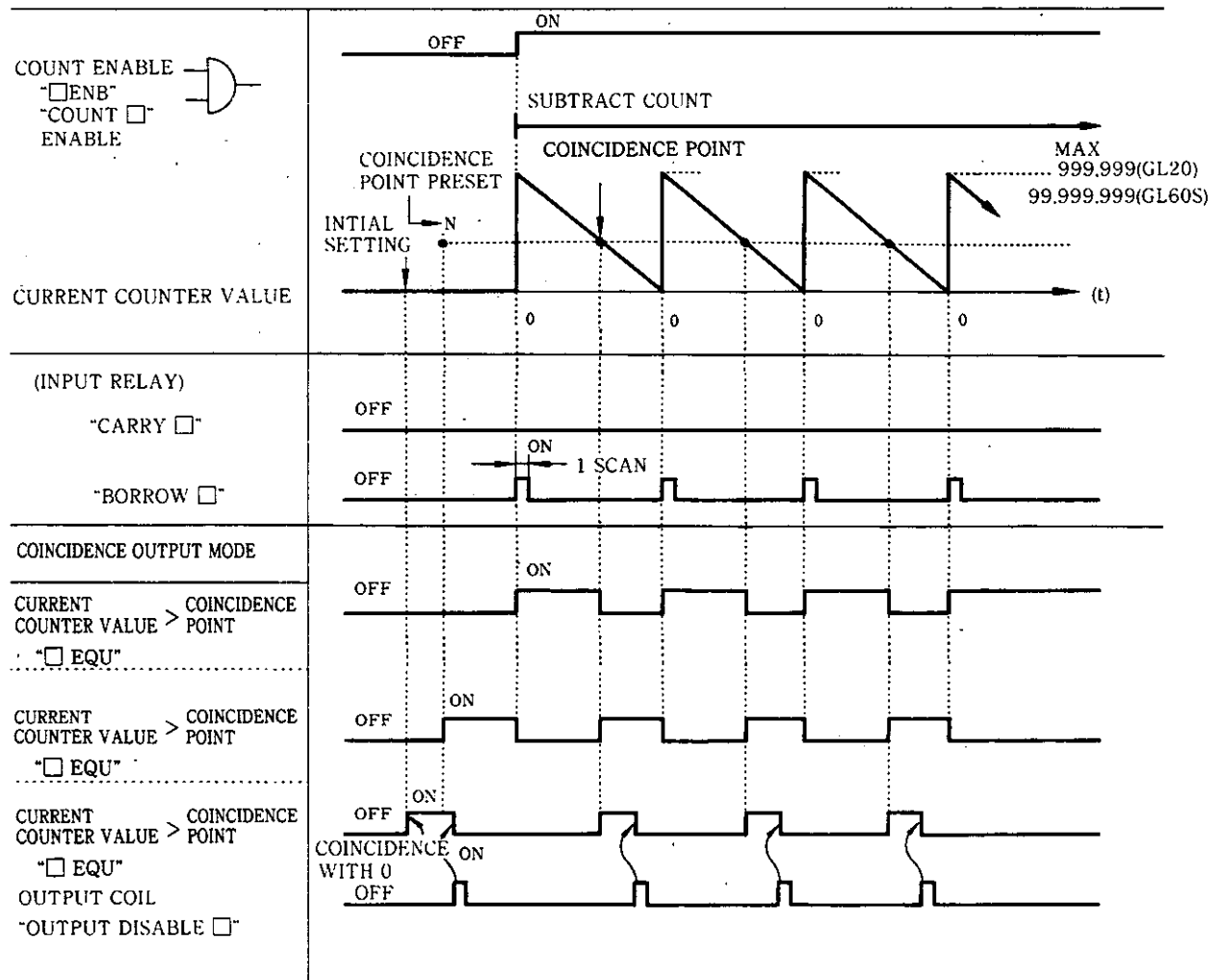


Note :

1. In the $>$ and $<$ modes the external coincidence output " $\square EQU$ " does not output 2n ON signal when the output coil "output disable \square " is set at the ON state.
2. In the $=$ mode, when "output disable \square " is set to on, " $\square EQU$ " ON is reset to off. Once " $\square EQU$ " is set to on, the ON state is retained until a reset signal by "output disable \square " is input.

Fig 4. 1 Basic Operation of Comparison Counter (ADD Count)

4. 1 COMPARISON COUNTER FUNCTION (Cont'd)



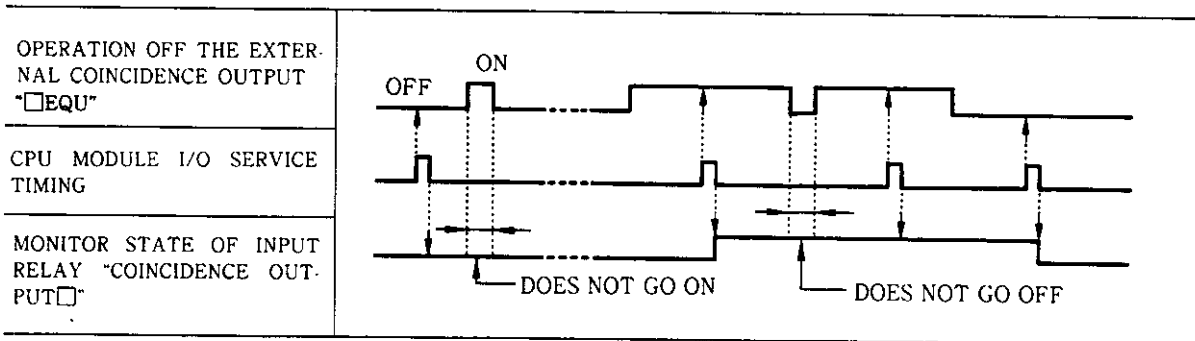
Note:

1. In the $>$ and $<$ modes the external coincidence output "EQU" does not output 2n ON signal when the output coil "output disable" is in the ON state.
2. In the $=$ mode, when the "output disable" is set to on, "EQU" ON is reset to off. Once "EQU" is turned to on, the ON state is retained until a reset signal by "output disable" ON is input.

Fig 4. 2 Basic Operation of Comparison Counter (SUBTRACT Count)

(2) Precautions for the Comparison Counter

- ① Current counter value and coincidence point preset value are reset to 0 when the unit is switched on, the module is reset, or when moved to the comparison counter mode during the initial setting.
- ② Under the current counter value with the $>$ coincidence point mode, when the maximum counter reading of 999, 999 (GL20) or 99, 999, 999 (GL60S) is set, condition for comparison is not satisfied, resulting in an unsatisfactory ON condition for the coincidence output.
- ③ Under the current value with the $<$ coincidence point mode, setting 0 to the coincidence point does not satisfy the ON condition.
- ④ While monitoring the state of external coincidence output by the input relay "coincidence output ", if duration of the external coincidence output ON/OFF is short, its state may not be reflected by the input relay. Set ON/OFF time longer than scanning time.

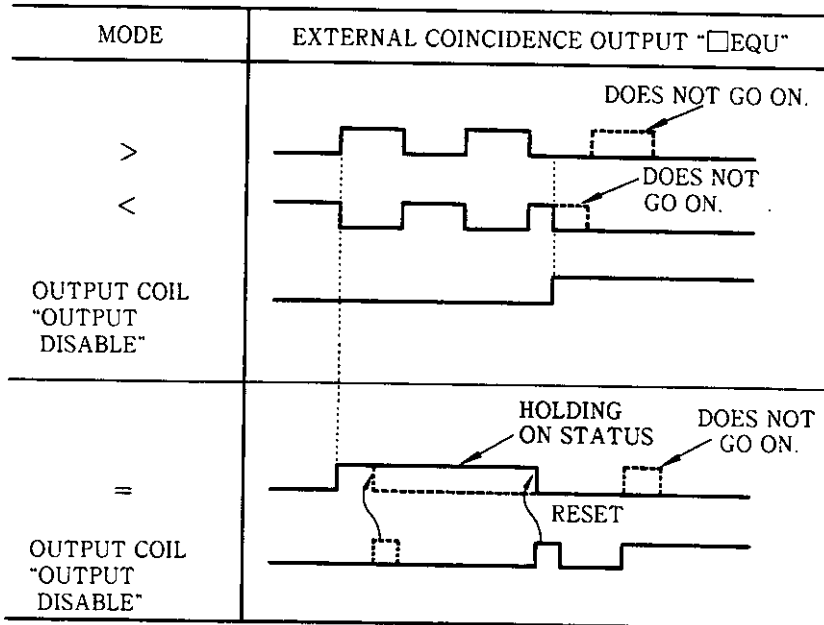


- ⑤ ON/OFF response of the external coincidence output is delayed a maximum of 5ms.
- ⑥ If a coincidence point (N) is set close to 0 or a maximum point, the following conditions may be observed.

4. 1 COMPARISON COUNTER FUNCTION (Cont'd)

MODE	ADDITION COUNT	SUBTRACT COUNT
SETTING OF A COINCIDENCE POINT	<p>MAX 999, 999 (GL20) 99, 999, 999 (GL60S)</p>	<p>MAX 999, 999 (GL20) 99, 999, 999 (GL60S)</p>
CURRENT COUNTER VALUE > COINCIDENCE POINT	<p>EXTERNAL COINCIDENCE OUTPUT</p> <p>ON DOES NOT GO OFF.</p>	<p>EXTERNAL COINCIDENCE OUTPUT</p> <p>DOES NOT GO ON. OFF</p>
CURRENT COUNTER VALUE < COINCIDENCE POINT	<p>EXTERNAL COINCIDENCE OUTPUT</p> <p>DOES NOT GO ON. OFF</p>	<p>EXTERNAL COINCIDENCE OUTPUT</p> <p>ON DOES NOT GO OFF.</p>
CURRENT COUNTER VALUE = COINCIDENCE POINT	<p>EXTERNAL COINCIDENCE OUTPUT</p> <p>ON RESPONSE IS LATE.</p>	<p>EXTERNAL COINCIDENCE OUTPUT</p> <p>ON RESPONSE IS LATE.</p>
CORRECTIVE MEASURE	<p>SET AT A COINCIDENCE POINT WHERE $t > 5\text{ms}$ IS SATISFIED. EXAMPLE: WHEN THE INPUT PULSE FREQUENCY IS 50kpps AND x1 SAMPLING COUNT, ITS COINCIDENCE POINT (N) IS SET AT:</p> $\frac{5\text{ms}}{1/50 \text{ kpps}} = 250 \text{ PULSES}$ $250 < N < (\text{MAX} - 250)$	

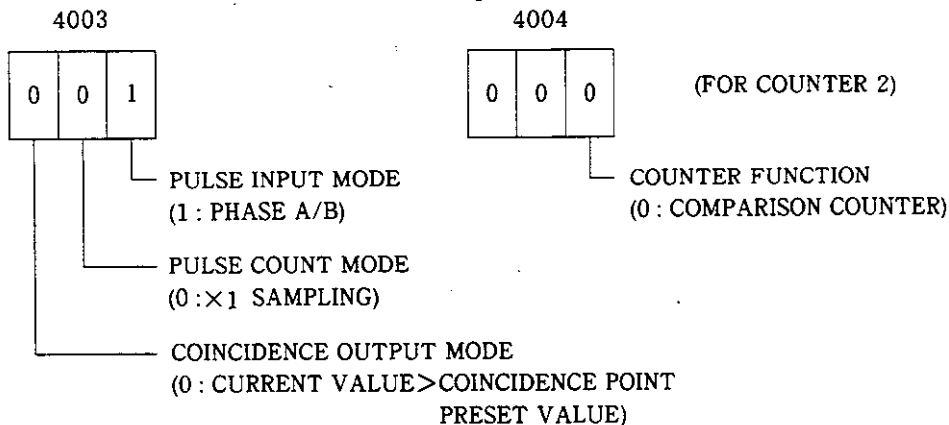
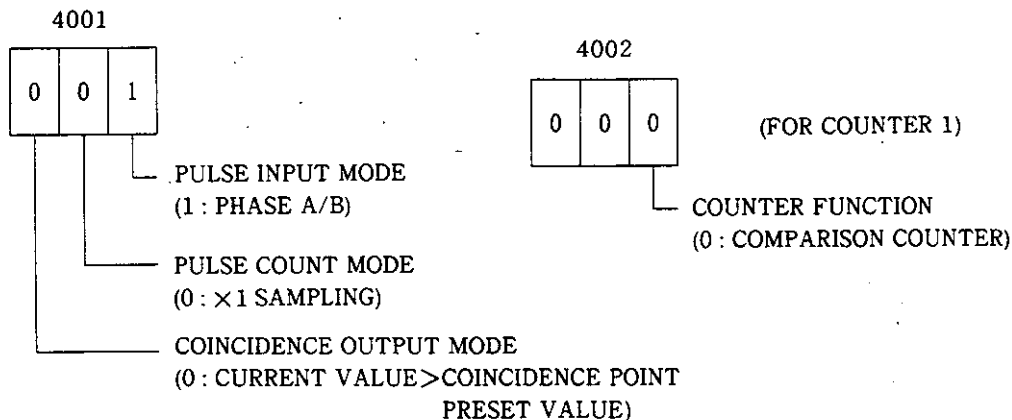
⑦ In the "<" and ">" modes the external coincidence output does not go on during the ON period of the output coil "output disable". In the = mode the ON output state is retained unless reset.



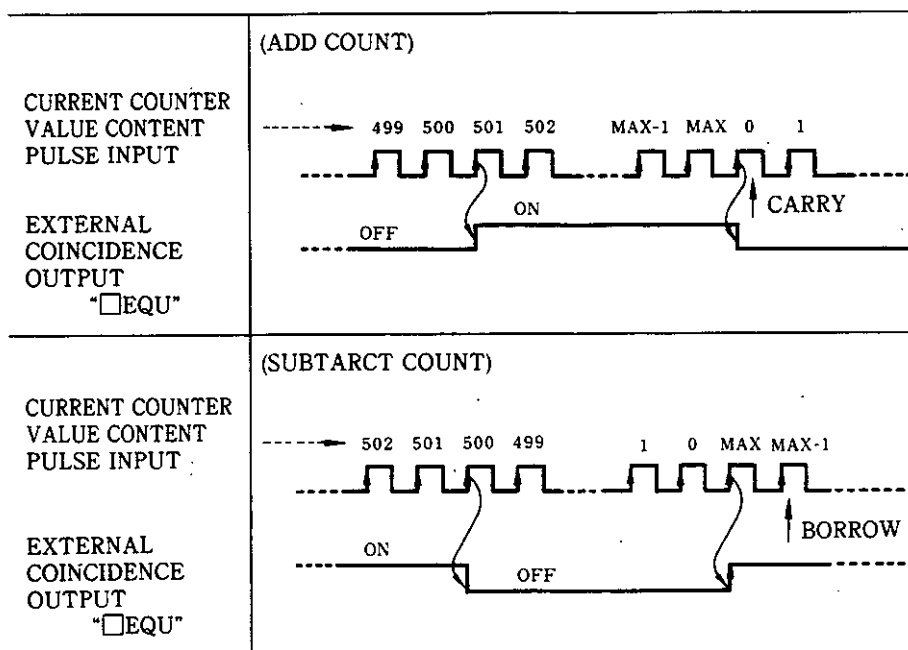
4. 1 COMPARISON COUNTER FUNCTION (Cont'd)

(3) Comparison Counter Operation and Ladder Circuits (6-digit Mode with GL20)

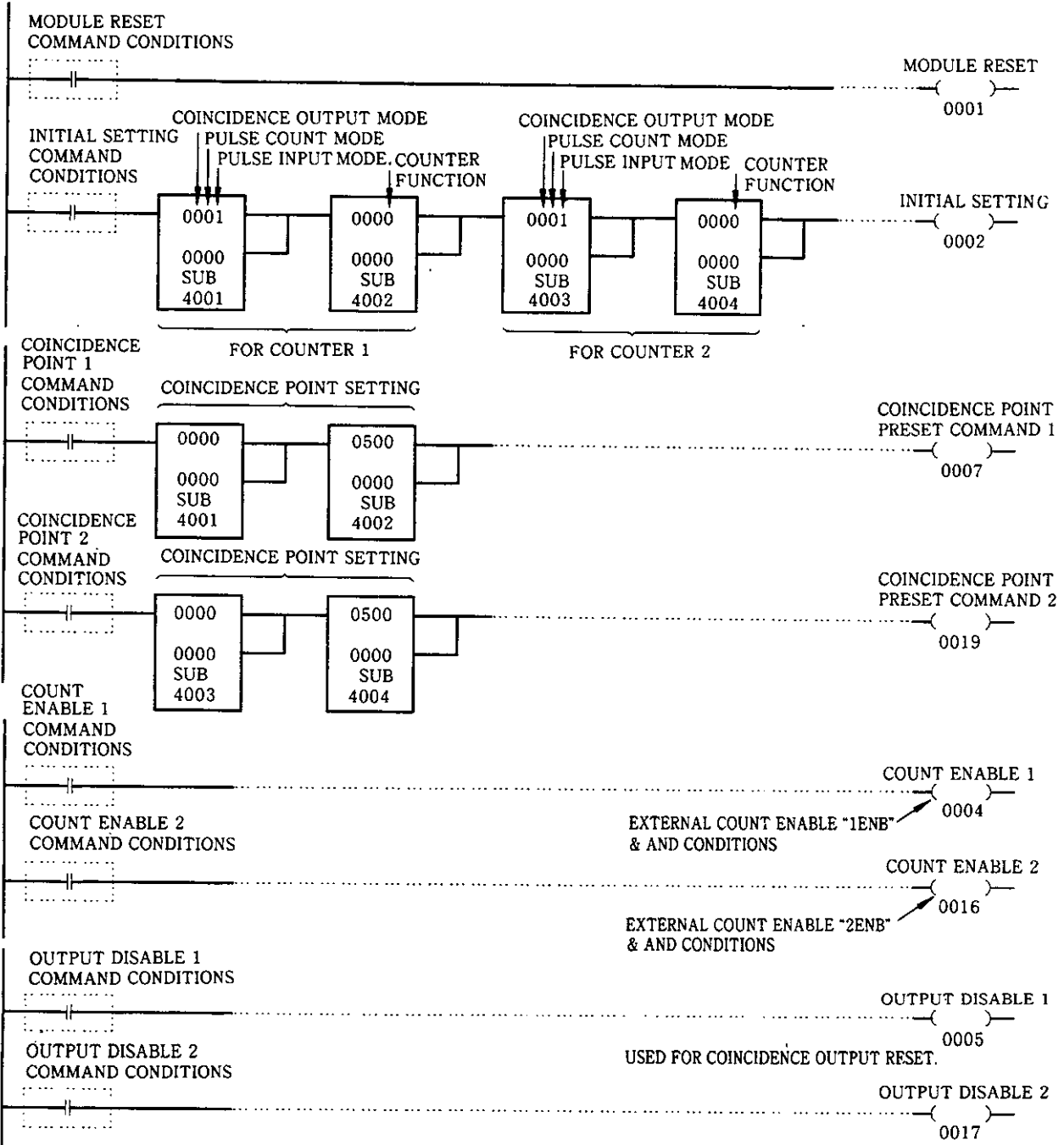
Initial settings are according to the diagrams below.



Coincidence preset value = 500



GL20 LADDER CIRCUIT



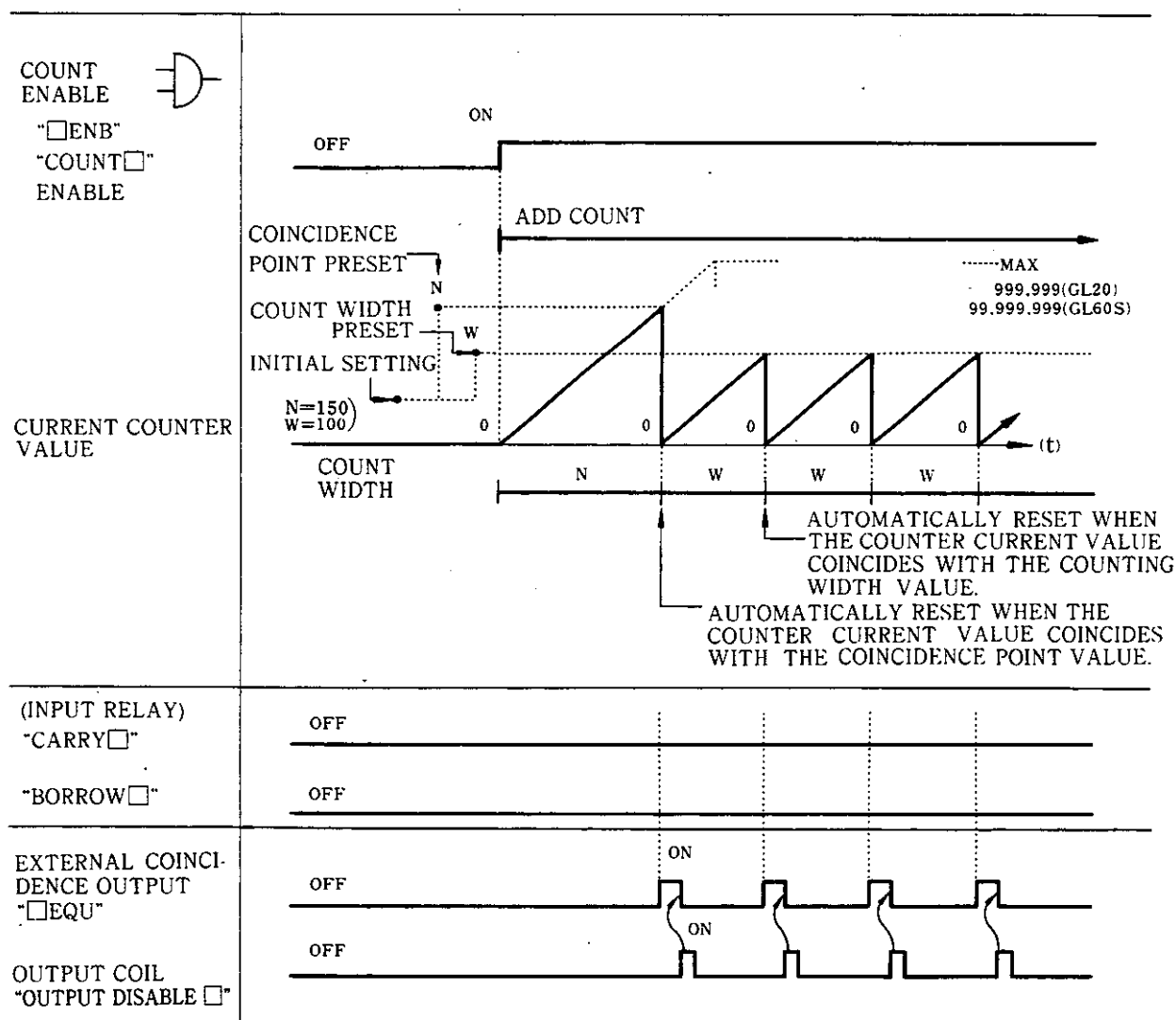
4. 2 CYCLIC COUNTER FUNCTION

(1) The cyclic counter is to repeat automatic resetting of the current counter value and pulse count from current value 0.

When the current counter value coincides with a coincidence preset value or a count width value the current counter value is automatically reset to 0, and the external coincidence signal "□EQU" is set to on. Repeat cycle depends on the count width.

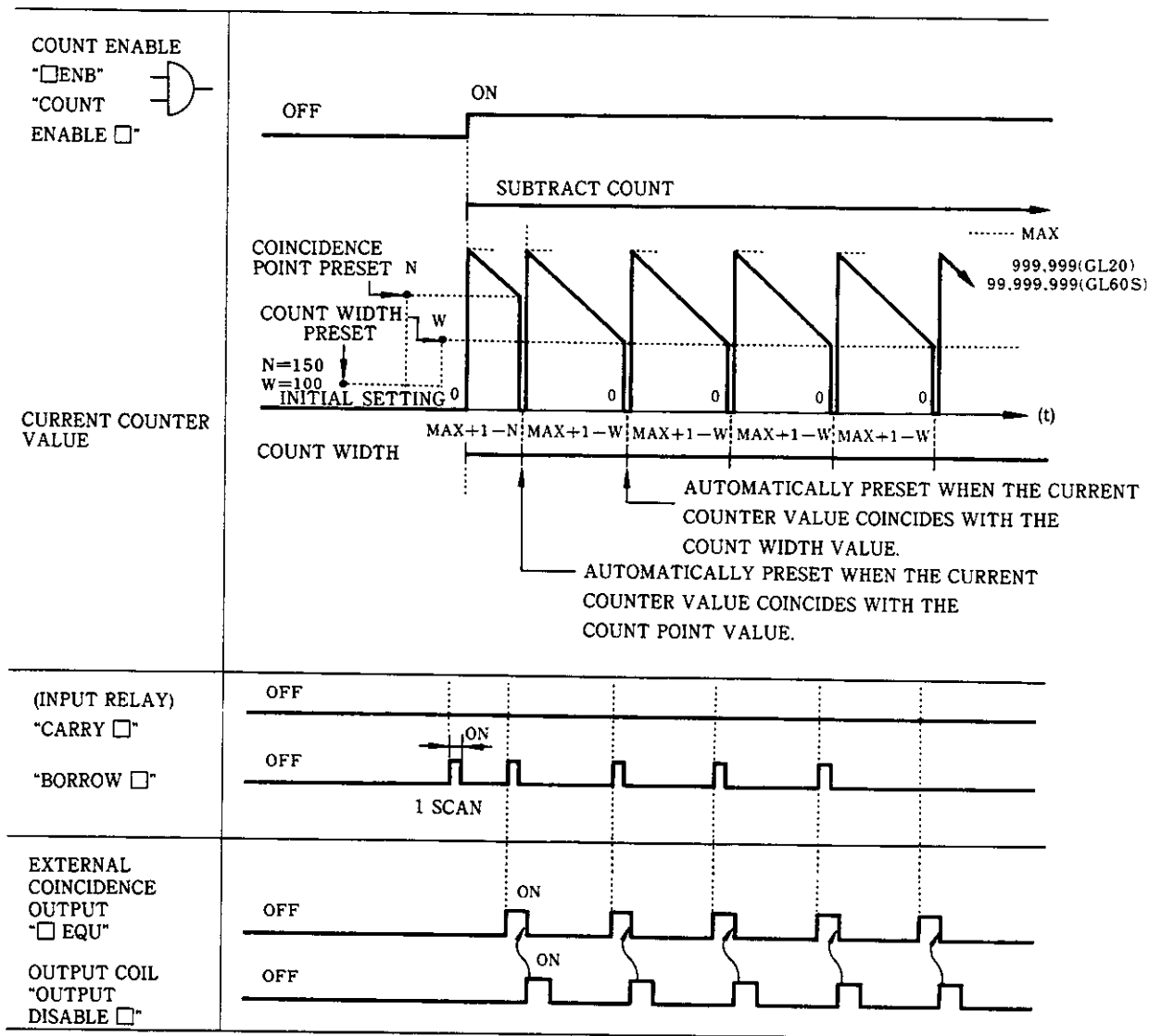
When the external coincidence output is turned on once, the ON output is retained. It can be reset by the ON signal of the output coil "output disable□".

Figs. 4. 3 and 4. 4 show basic operation of the cyclic counter.



Note: When the cyclic counter is specified by initial setting, the current counter value is automatically set to 0, and coincidence point (N) and count width (W) to the default value of 100.

Fig. 4. 3 Basic Operation of Cyclic Counter (ADD)



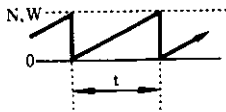
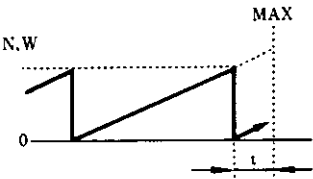
Note: When the cyclic counter is specified by initial setting, coincidence point (N) and count width (W) to the default value of 100.

Fig. 4. 4 Basic Operation of Cyclic Counter (SUBTRACT Count)

4.2 CYCLIC COUNTER FUNCTION (Cont'd)

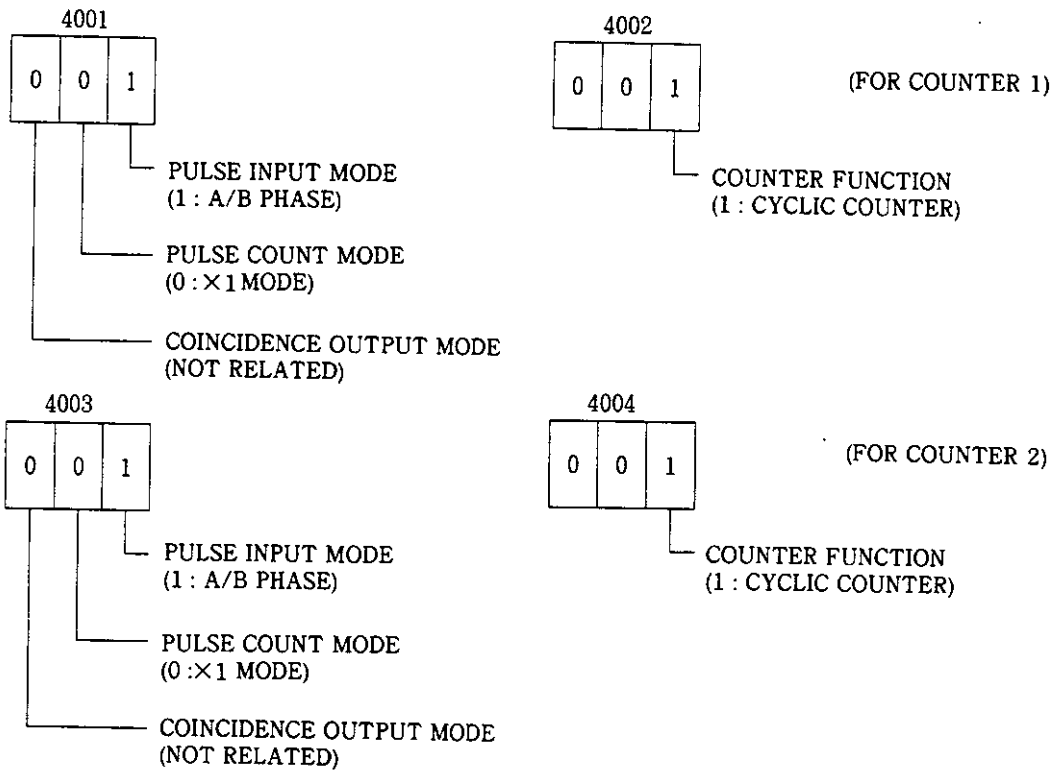
(2) Precautions for Cyclic Counter

- ① Coincidence preset value (N) and count preset value (W) set a point at $t = 5\text{ms}$ or further in current counter value.

<p>PULSE COUNT</p> <p>COUNTER CURRENT VALUE</p>	<p>CLOSE TO 0 POINT</p> 	<p>CLOSE TO MAX POINT</p> 
<p>REMEDIES</p>	<p>SET COINCIDENCE POINT AND COUNT WIDTH TO SATISFY $t > 5\text{ms}$. (EXAMPLE) WHEN THE INPUT PULSE FREQUENCY IS 50kpps WITH 4-TIME COUNT,</p> $\frac{5\text{ms}}{1/(50 \text{ kpps} \times 4)} = 1000 \text{ PULSES}$ <p>WHERE $1000 < N, W < (\text{MAX} - 1000)$</p>	

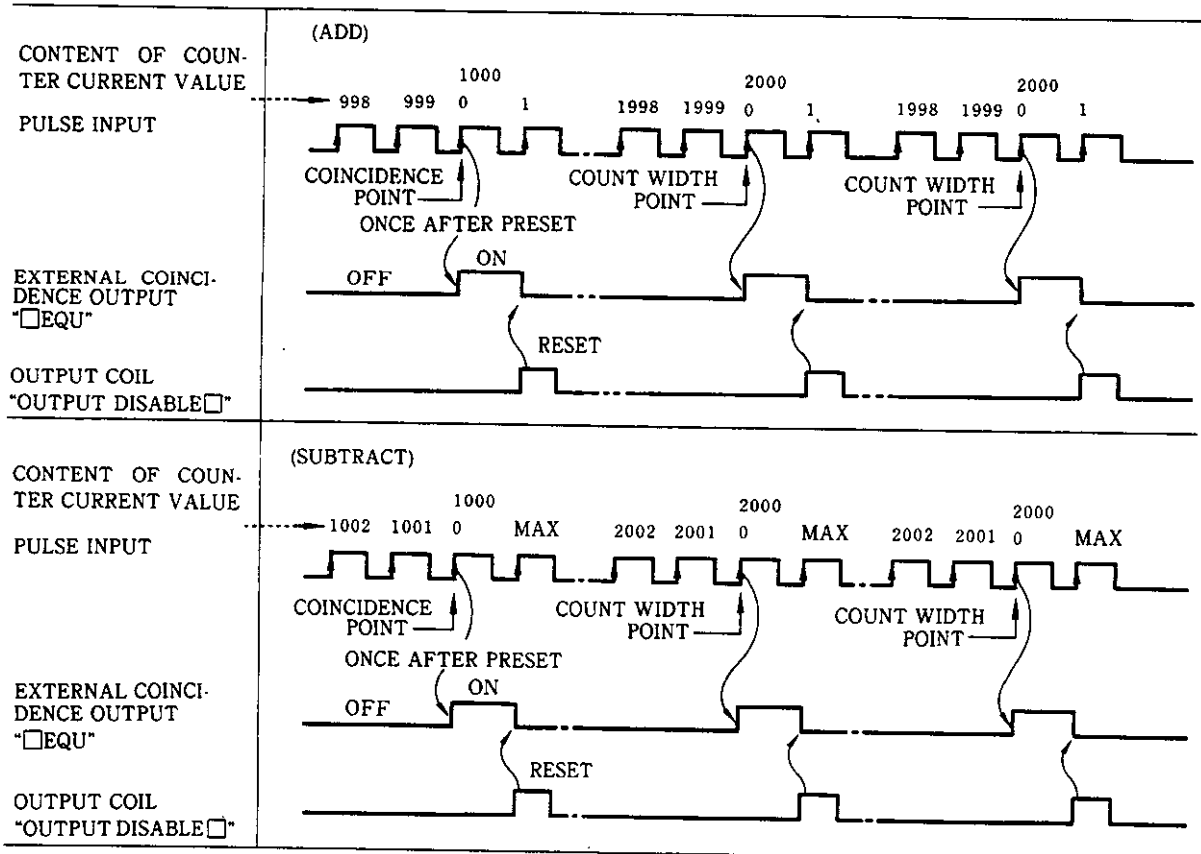
- ② When count width preset value is set at 0, current counter value stays at 0. Neither ADD or SUBTRACT count is executed. External coincidence output retains the ON output.
- ③ ON/OFF response of the external coincidence output is delayed 5ms maximum.
- ④ While external reset or current value reset is ON count operation is stopped.

(3) Cyclic Counter Operation and Ladder Circuits (6-digit Mode with GL20)
 Initial settings are according to diagrams below.



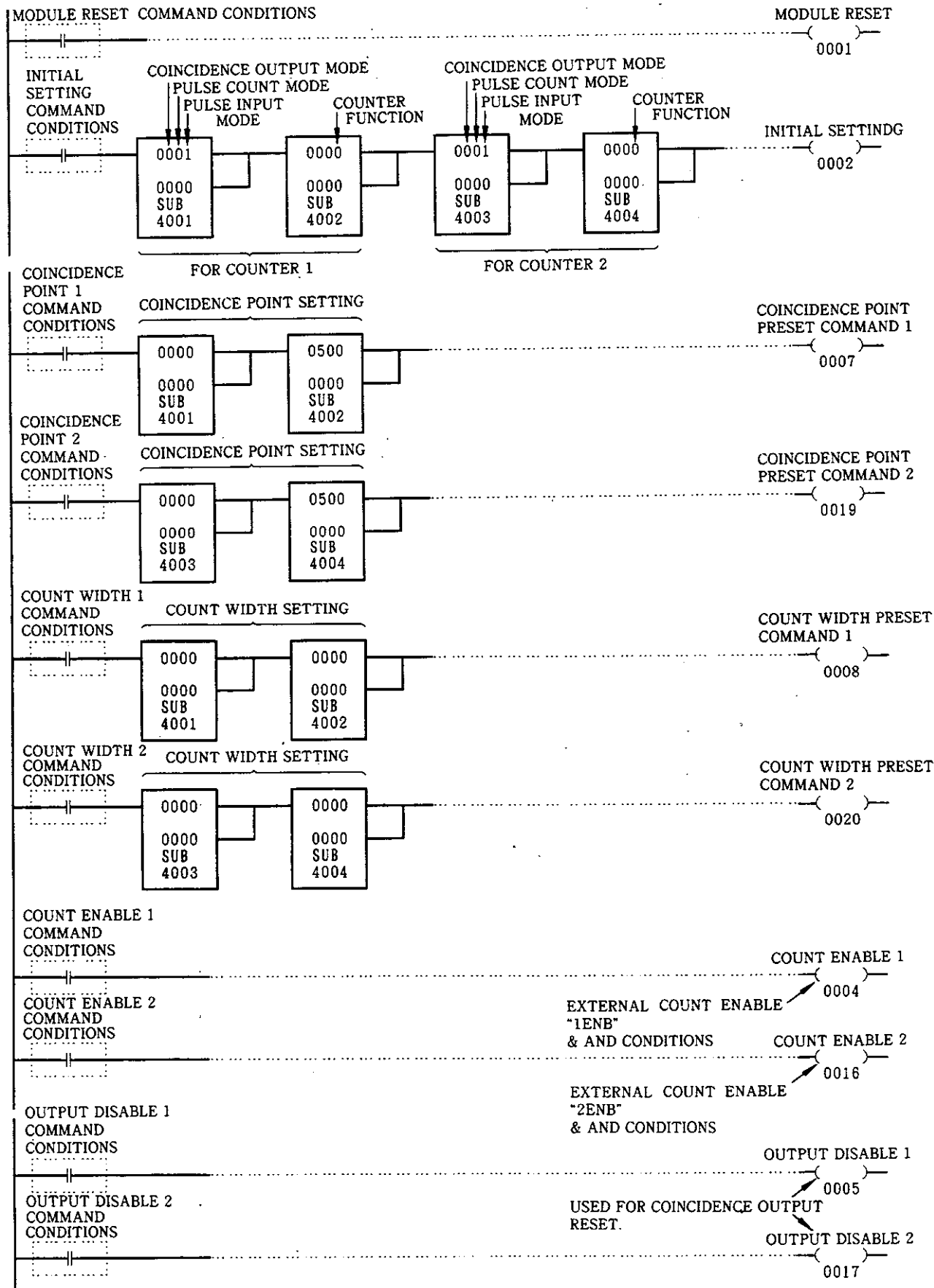
COINCIDENCE PRESET VALUE = 1000
 COUNT WIDTH PRESET VALUE = 2000

MAX 999,999 (GL20)
 99,999,999 (GL60S)



4. 2 CYCLIC COUNTER FUNCTION (Cont'd)

GL20 LADDER CIRCUIT



4.3 SAMPLING COUNTER FUNCTION

(8) The current counter value are latched everytime external sampling signals are received, and the latched and up-to-date current counter values are stored in a specified input register.

Contents of counter 1 are stored in the first and second input registers ; those of counter 2 in the third and fourth input registers.

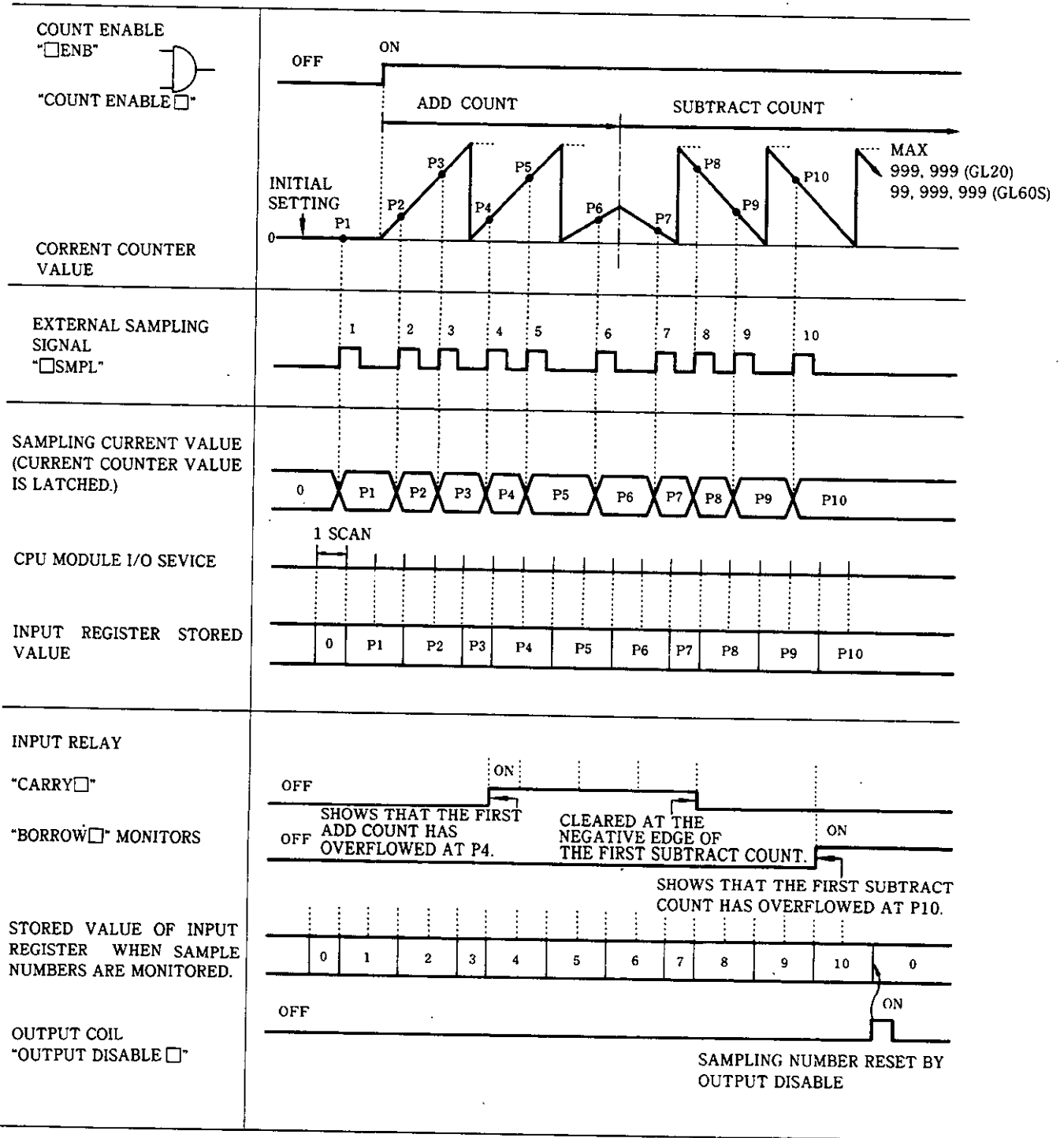


Fig. 4.5 Basic Operation of Sampling Counter

4. 3 SAMPLING COUNTER FUNCTION (Cont'd)

(2) Period T of External Sampling ("□SMPL")

① Period T of the external sampling should be more than 10ms and, at the same time, should satisfy the following conditions.

Mode	Period	f=Input Pulse Frequency k=Multiplier (×1, ×2, ×4)
6-digit Mode (GL20)		$T \leq (2^{19}-1)/f \cdot k = 524287/f \cdot k$ <p>Example : when f=50kpps</p> <p>×1 count : 10ms \leq T \leq 10s ×2 count : 10ms \leq T \leq 5s ×4 count : 10ms \leq T \leq 2.5s</p>
8-digit Mode (GL60S)		$T \leq (2^{23}-1)/f \cdot k = 8388607/f \cdot k$ <p>Example : when f=50kpps</p> <p>×1 count : 10ms \leq T \leq 167s ×2 count : 10ms \leq T \leq 83s ×4 count : 10ms \leq T \leq 41s</p>

② The ON response time of the external sampling signal is less than 1ms, and OFF response time less than 2ms. Pulse width of the sampling signal should be set to more than 5ms.

(3) Precautions for the Sampling Counter

① When the sampling counter is specified by initial setting, current counter value becomes 0. Carry and borrow flags become OFF.

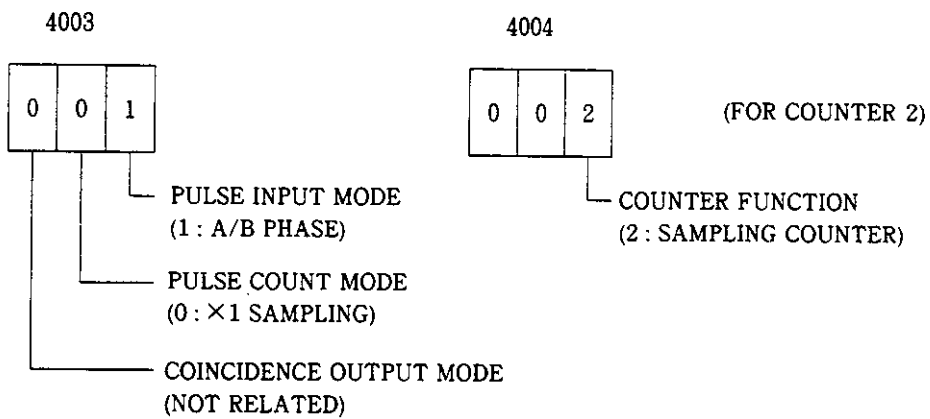
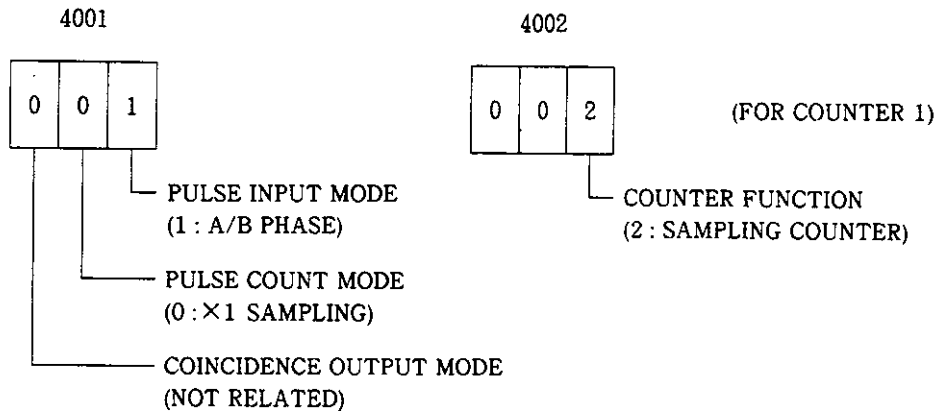
② When the output coil "current value reset□" is turned on, current sampling value and current counter value are made 0. Carry and borrow flags become OFF.

③ If current value is preset during pulse count, current sampling value and current counter value become the same as the current preset values.

④ Number of samplings is reset by the output coil "output disable□".

⑤ If external sampling signal is received at shorter intervals than the scanning time of the CPU module, current sampling value and sampling frequency are stored in the input registers.

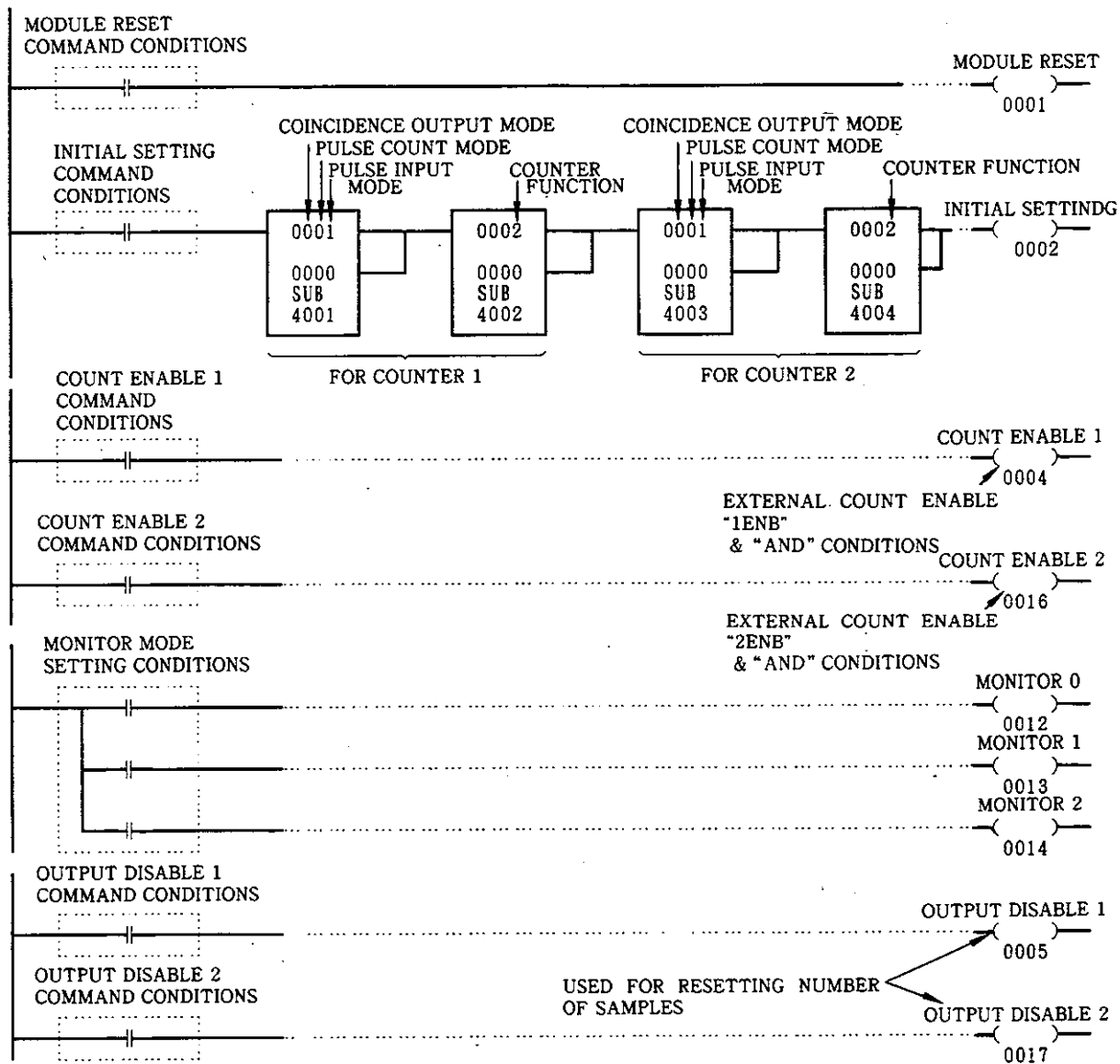
(4) Sampling Counter Operation and Ladder Circuits (6-digit Mode with GL20)
 Initial settings are according to the diagrams below.



Current sampling value or sampling number is monitored. Monitor data is stored in the first and second input registers allocated for counter 1, and third and fourth for counter 2.

4.3 SAMPLING COUNTER FUNCTION (Cont'd)

GL20 LADDER CIRCUIT



4. 4 MEMORY COUNTER FUNCTION

(1) As external sampling signal is received the current counter value is latched and stored in the built-in data memory in order of receiving. Up to 999 data can be stored, and the stored data in any address can be read at a specified input register by output coil "pointer command□".

Once sampling of specified frequencies is completed by output coil "stored number of preset command□" the external coincidence output signal "□EQU" is set ON.

When the output coil "output disable" is turned on, stored data is cleared, sample store number is reset, and "□EQU" output is switched off. Fig.4. 6 shows basic operation of memory counter.

4.4 MEMORY COUNTER FUNCTION (Cont'd)

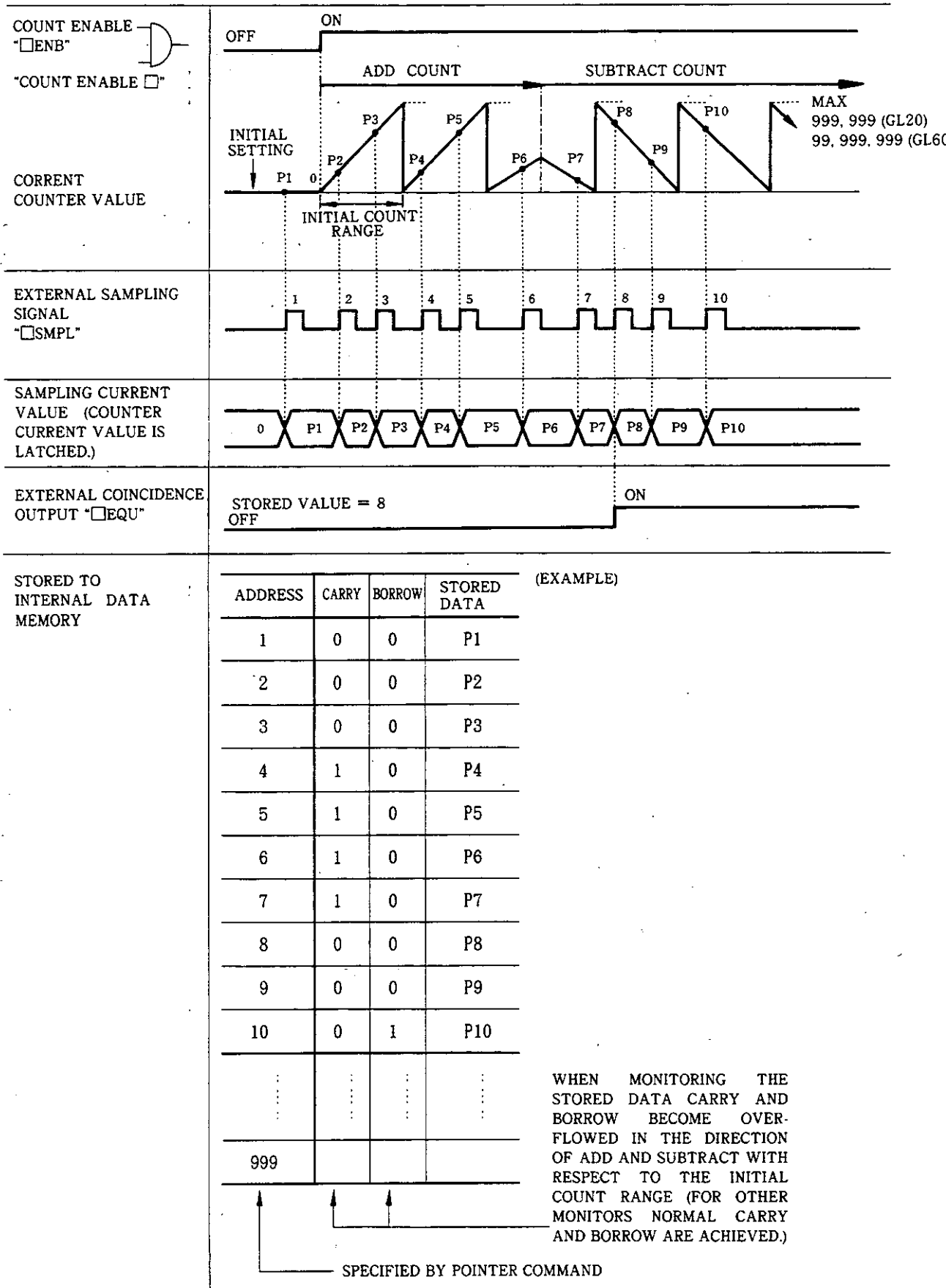


Fig. 4.6 Basic Operations of Memory Counter

(2) Precautions for the Memory Counter

- ① When the memory counter is specified by initial setting, current counter value, stored number preset value and sample stored number become 0.
- ② When the sample stored number reaches 999 no more sampling is processed.
- ③ Monitor of the stored data, when pointer command = 0, is always 0.
- ④ When the stored number preset value = 0, the external coincidence output is not turned on.
- ⑤ Period T of the external sampling should be more than 10ms and, at the same time, should satisfy the following conditions.

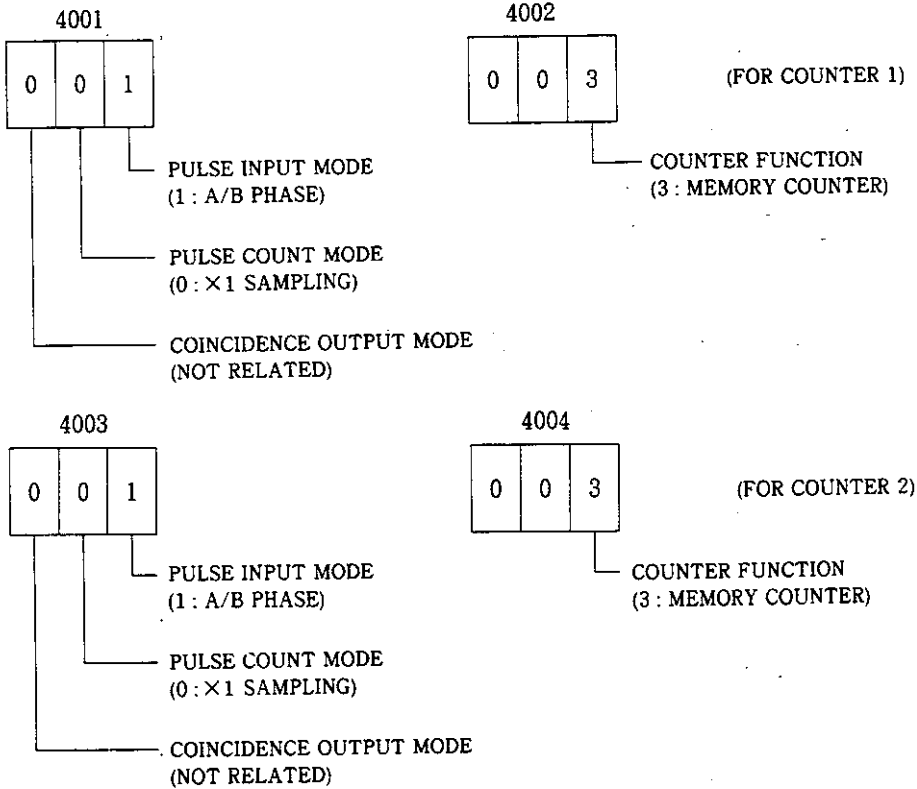
Period Mode	f=Input Pulse Frequency k=Multiplier (x1, x2, x4)
6-digit Mode (GL20)	$T \leq (2^{19}-1)/f \cdot k = 524287/f \cdot k$ <p>Example : when f=50kpps</p> <p>x1 count : 10ms $\leq T \leq$ 10s x2 count : 10ms $\leq T \leq$ 5s x4 count : 10ms $\leq T \leq$ 2.5s</p>
8-digit Mode (GL60S)	$T \leq (2^{23}-1)/f \cdot k = 8388607/f \cdot k$ <p>Example : when f=50kpps</p> <p>x1 count : 10ms $\leq T \leq$ 167s x2 count : 10ms $\leq T \leq$ 83s x4 count : 10ms $\leq T \leq$ 41s</p>

- ⑥ The ON response time of the external sampling signal is less than 1ms, and the OFF response time less than 2ms. Pulse width of the sampling signal should be set to more than 5ms.

4. 4 MEMORY COUNTER FUNCTION (Cont'd)

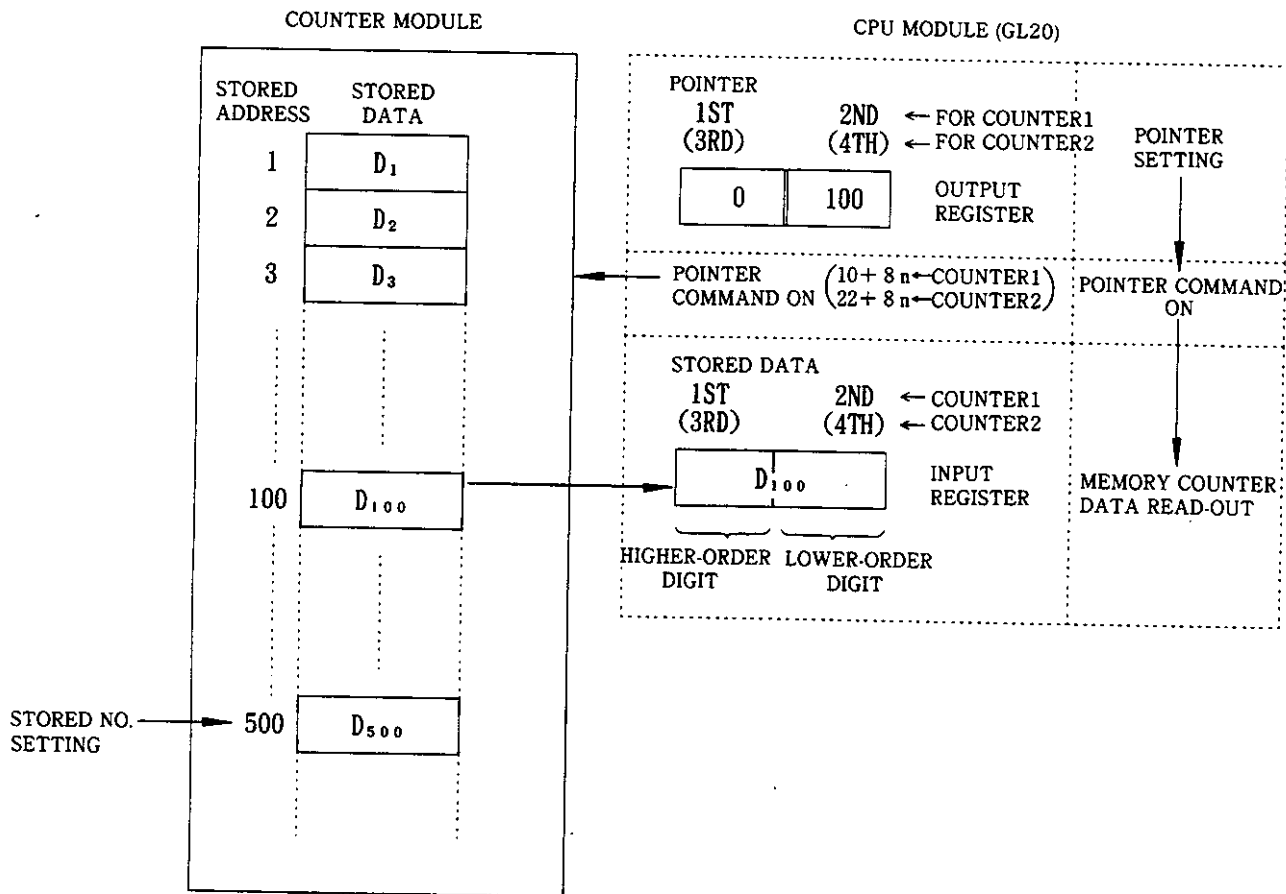
(3) Memory Counter Operation and Ladder Circuits (6-digit Mode with GL20)

Initial settings are according to the diagrams below.



The number of stored sampling data is 500, and read out stored address by pointer command is 100. Contents of the monitor data in counter 0 are stored in the first and second allocated input registers, and contents of counter 2 in the third and fourth.

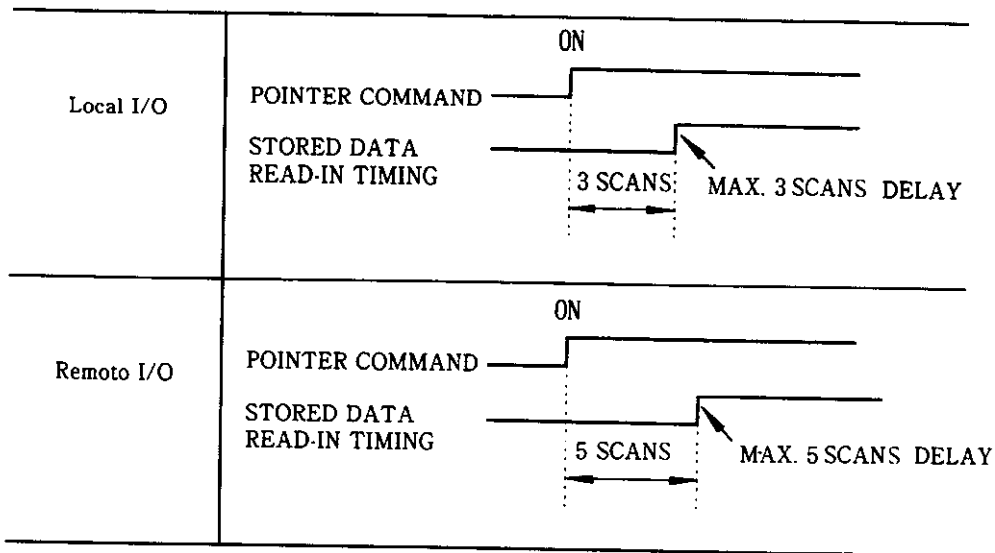
During pointer command monitor, output coils "monitor 0", "monitor 1" and "monitor 2" are turned off.



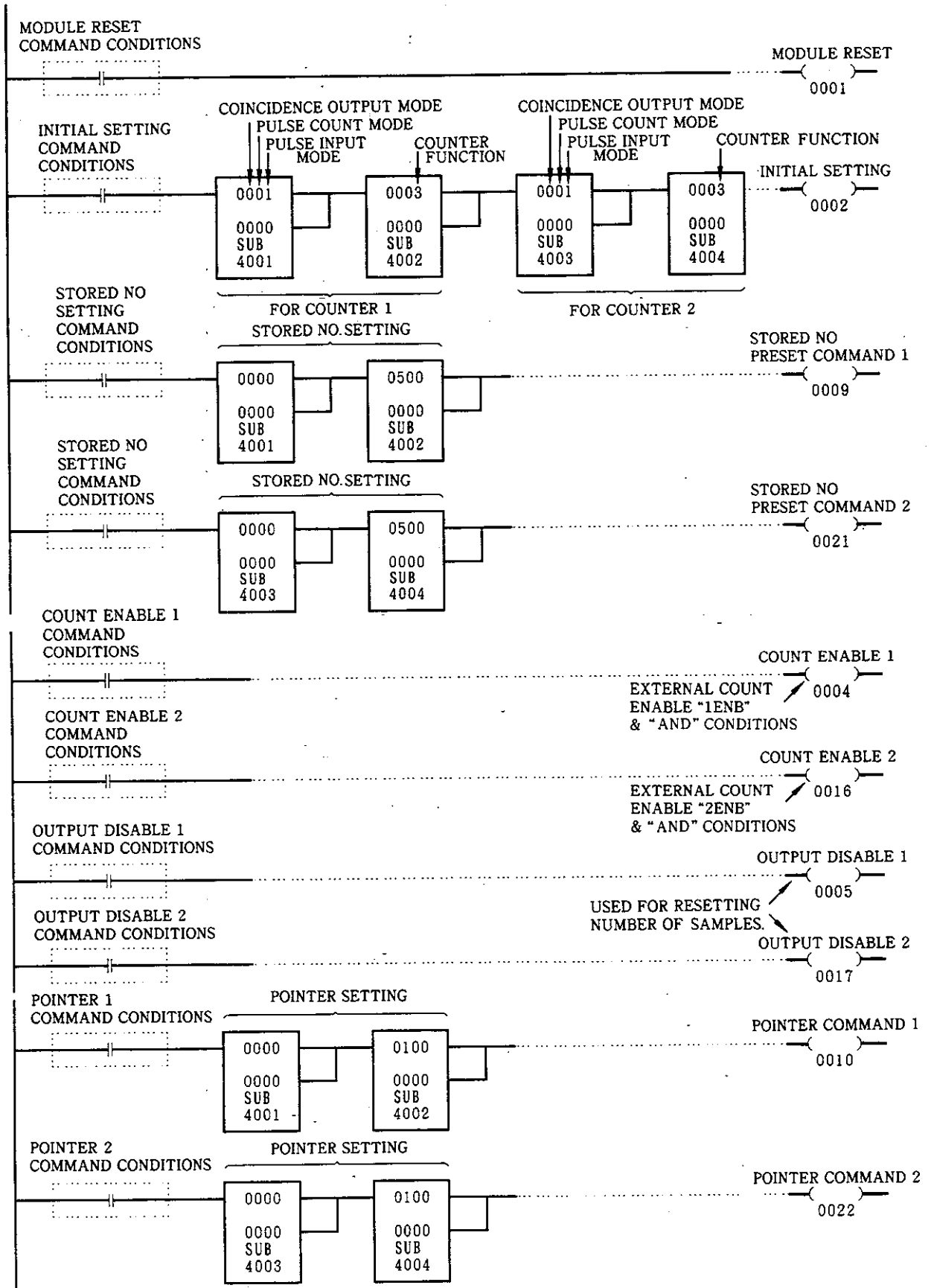
Note

Stored data are being read out only while pointer command is ON.
 Current counter value is entered in input register when pointer command is OFF.

Scan Timing of Pointer Command ON and Stored Data Read-Out



GL20 LADDER CIRCUIT



5. INTERNAL INTERFACE

I/O interface between CPU module and B2801 is explained.

5.1 ALLOCATION OF CPU MODULE

For I/O interface between CPU module and B2801, output coils, input relays, I/O registers are used. Table 5. 1 shows the number of I/O points allocated for CPU module. I/O register allocation is by binary codes.

Table 5. 1 Allocation Points to CPU Module

I/O Allocation	NO. of I/O	Signal Flow	
		CPU Module	B2801
Output Coil	24 or 16 points	→	→
Input Relay	16 or 8 points	←	←
Output Register	4	→	→
Input Register	4	←	←

5. 2 OUTPUT COIL (CONTROL SIGNAL) CPU MODULE TO B2801

(1) Output Coils

There are 24 (or 16) output coils which comprise control signals from CPU module to the B2801. If counter 2 is not used, 16-point allocation is acceptable, but simultaneous use of counters 1 and 2 always requires 24-point allocation. Table 5. 2 shows a list of output coils.

Table 5. 2 Output Coil List

GL20	GL60	Signal Name
0001+8n	00001+8n	Module reset
0002+8n	00002+8n	Initial setting
0003+8n	00003+8n	Current value reset 1
0004+8n	00004+8n	Count enable 1
0005+8n	00005+8n	Output disable 1
0006+8n	00006+8n	Current value preset command 1
0007+8n	00007+8n	Coincidence point preset command 1
0008+8n	00008+8n	Count width preset command 1
0009+8n	00009+8n	Stored number preset command 1
0010+8n	00010+8n	Pointer command
0011+8n	00011+8n	Forced coincidence output
0012+8n	00012+8n	Monitor 0
0013+8n	00013+8n	Monitor 1
0014+8n	00014+8n	Monitor 2
0015+8n	00015+8n	Current value reset 2
0016+8n	00016+8n	Current enable 2
0017+8n	00017+8n	Output disable 2
0018+8n	00018+8n	Current value preset command 2
0019+8n	00019+8n	Coincidence point preset command 2
0020+8n	00020+8n	Count width preset command 2
0021+8n	00021+8n	Stored number preset command 2
0022+8n	00022+8n	Pointer command 2
0023+8n	00023+8n	Forced coincidence output 2
0024+8n	00024+8n	For future use

Exclusively for Counter 1

Exclusively for Counter 2

□ Indicate reference number for allocating output coils.
n = 0, 1, 2, ...

(2) Output Coils

The 24 output coils produce control signals as detailed in Table 5. 3. Except monitors 0, 1 and 2, numbers after names of signals indicate that they are control signals exclusive to counters 1 and 2, respectively.

Table 5. 3 Output Coil Signal

Reference No.		Name	Description
GL20	GL60S		
0001+8n	00001+8n	Module reset	Module reset command. When the B2801 receives a module reset signal, internal RAM, external I/O signals are initialized. Counters 1 and 2 show default values of initial setting (refer to Par. 4. 4. 1). Effective when OFF to ON.
0002+8n	00002+8n	Initial setting	Initial setting command of the B2801 (initial values are set to output registers). Sets counter function of the module. Effective when OFF to ON. Both "count enable 1" and "count enable 2" coils should be OFF.
0003+8n 0015+8n	00003+8n 00015+8n	Current value reset 1 and 2	While "current value reset" is ON, current value of the relevant counter becomes 0. Also, count operation is stopped. Effective at ON.
0004+8n 0016+8n	00004+8n 00016+8n	Count enable 1 and 2	When both "count enable□" and external count enable signal "□ENB" are ON, the relevant counter performs pulse count. Effective at ON.
0005+8n 0017+8n	00005+8n 00017+8n	Output disable 1 and 2	While "output disable□" is ON, the external coincidence output signal "□ENB" does not output ON. Depending on setting of the counter function mode they become a control signal to reset "□EQU" (refer to Par. 3). Effective at ON.
0006+8n 0018+8n	00006+8n 00018+8n	Current value preset commands 1 and 2	Preset command of current counter value. They preset output register values to current counter values. Effective when OFF to ON.
0007+8n 0019+8n	00007+8n 00019+8n	Coincidence point preset commands 1 and 2	Preset command for coincidence point of a counter. Used with the comparison counter and cyclic counter function modes. Invalid with other modes. Coincidence point should be set in output registers. Effective when OFF to ON.
0008+8n 0020+8n	00008+8n 00020+8n	Counting width preset commands 1 and 2	Used with the cyclic counter mode. Invalid with other modes. Count width of current value to operate cyclic count is specified. Count width should be set in output registers. Effective when OFF to ON.

(Cont'd)

5. 2 OUTPUT COIL (CONTROL SIGNAL) CPU MODULE TO B2801 (Cont'd)

Table 5. 3 Output Coil Signal (Cont'd)

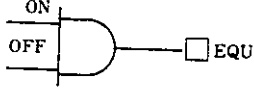
Reference No.		Name	Description
GL20	GL60S		
0009+8n 0021+8n	00009+8n 00021+8n	Stored number Preset commands 1 and 2	Used with the memory counter function mode. Invalid with other modes. Instruction to set stored number of sampling data. Stored number should be set in output registers. Effective when OFF to ON.
0010+8n 0022+8n	00010+8n 00022+8n	Pointer commands 1 and 2	Used with the memory counter function mode. Invalid with other modes. Command to specify a data stored address when reading out stored sampling data. Read out address should be set in output registers. Effective during ON.
0011+8n 0023+8n	00011+8n 00023+8n	Forced coincidence outputs 1 and 2	Control signal to force external coincidence output signal "□ EQU" to ON. Effective during the control signal is ON. It forms AND condition with "output disable". FORCED COINCIDENCE OUTPUT 1 □ OUTPUT DISABLE □ 
0012+8n 0013+8n 0014+8n	00012+8n 00013+8n 00014+8n	Monitor 0 1 2	Common to counters 1 and 2. Various monitor data are set to input registers depending on combinations. Even if the combinations are the same, different counter function modes will provide different monitor results.

Table 5. 4 Counter Function Modes and Monitor Description

Name			Counter Function Modes and Monitor Results				
Monitor 1	Monitor 2	Monitor 3	Comparison counter	Cyclic counter	Sampling counter	Memory counter	
0	0	0	Current counter value	Current counter value	Current Sampling value	Stored data [†]	
1	0	0	Current preset value	Current preset value	Current preset value	Current preset value	
0	1	0	Coincidence point preset value	Coincidence point preset value	Current counter value	Current counter value	
1	1	0	Current counter value	Count width preset value		Sample number [*]	Sample stored number [‡]
0	0	1		Current counter value			
1	0	1		Pointer command Setting value			
0	1	1	Initial setting value	Initial setting value	Initial setting value	Initial setting value	
1	1	1			Initial setting value	Initial setting value	

* Shows numbers of sampling. It is reset by "initial setting" ON or "output disable□" ON.

† Stored data - Stored data of the memory counter are shown during the ON period of pointer instruction. When it turns to OFF current counter value is shown.

‡ Stored sample number - Shows stored number of the memory counter data. It is reset by "initial setting" ON or "output disable□" ON.

(3) Conditions for Output Coils

Tables 5. 5 and 5. 6 show conditions for output coils for all counter function modes. Commands which do not satisfy ON or OFF conditions of the output coils are errors. Commands which are not related to the counter functions are disregarded.

Output coils which are exclusive to counter 1 or 2 do not interrupt with each other. For commands of initial settings, both "count enable 1" and "count enable 2" should be OFF.

Table 5. 5 Output Coil Conditions for Comparison Counter and Cyclic Counter

Counter Function	Cyclic Counter Function										
	Comparison Counter Function										Count width preset <input type="checkbox"/> command
Output Coil Signal	Module reset	Initial setting	Current value reset	Count enable <input type="checkbox"/>	Output disable <input type="checkbox"/>	Current value preset command <input type="checkbox"/>	Coincidence point preset command <input type="checkbox"/>	Forced coincidence output <input type="checkbox"/>	Monitors 0 to 2		
Module Reset											
Initial Setting	—			Both 1 and 2 0		Both 1 and 2 —	Both 1 and 2 —			Both 1 and 2 —	
Current Value Reset	—		①								
Count Enable	—			①							
Output Disable	—				①						
Current Value Preset	—	—					—			—	
Coincidence Point Preset	—	—				—				—	
Forced Coincidence Output	—							①			
Monitor	—								Com- bination of 1 and 0		
Counter Width Preset Command	—	—				—	—				

Note: Symbols in table above mean the followings

1: ON, 0: OFF, : OFF→ON, —: no status change, Blank space: disregarded,
① & : indicate coils which are made effective after conditions of other coils are met.

5. 2 OUTPUT COIL (CONTROL SIGNAL) CPU MODULE TO B2801 (Cont'd)

Table 5. 6 Output Coil Conditions for Sampling Counter and Memory Counter

Counter Function	Memory Counter Function										
	Sampling Counter Function										Pointer command
Output Coil Signal Module Operation	Module reset	Initial setting	Current value reset	Count enable <input type="checkbox"/>	Output dis-able <input type="checkbox"/>	Current value preset command <input type="checkbox"/>	Forced coincidence output <input type="checkbox"/>	Monitors 0 to 2	Stored Number Preset command		
Module Reset											
Initial Setting	—			Both 1 and 2 0		Both 1 and 2 —			Both 1 and 2 —	Both 1 and 2 —	
Current Value Reset	—	—	①								
Count Enable	—			①							
Output Disable	—				①						
Current Value Preset	—	—							—	0	
Forced Coincidence Output							①				
Monitors 0 to 2	—							Combina-tion of 1 and 0			
Stored Number Preset	—	—				—				0	
Pointer Command	—	—				0	All of 0, 1, 2	0			①

Note : Symbols in table above mean the followings

1 : ON, 0 : OFF, : OFF→ON, — : no status change. Blank space : disregarded.

① & : indicate coils which are made effective after conditions of other coils are met.

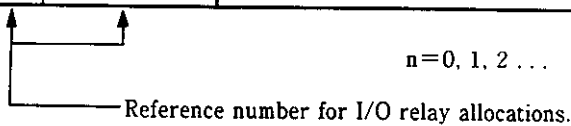
5. 3 INPUT RELAYS (CONTROL SIGNAL) B2801 TO CPU MODULE

(1) Input Relays

Sixteen (or eight) input relays are used to form control signals from the B2801 to CPU module. Eight-point allocation is acceptable if counter 2 is not used. Sixteen-point allocation must be made when counters 1 and 2 are used simultaneously. Table 5. 7 shows a list of input relays.

Table 5. 7 Input Relay List

GL20	GL60S	Signal Name	
1001+8n	10001+8n	READY	
1002+8n	10002+8n	Preset ACK1	
1003+8n	10003+8n	Preset NAK1	
1004+8n	10004+8n	Carry 1	} Exclusively for Counter 1
1005+8n	10005+8n	Borrow 1	
1006+8n	10006+8n	Coincidence output 1	
1007+8n	10007+8n	Not used	
1008+8n	10008+8n	Not used	
1009+8n	10009+8n	Preset ACK2	} Exclusively for Counter 2
1010+8n	10010+8n	Preset NAK2	
1011+8n	10011+8n	Carry 2	
1012+8n	10012+8n	Borrow 2	
1013+8n	10013+8n	Coincidence output 2	
1014+8n	10014+8n	Not used	
1015+8n	10015+8n	Not used	
1016+8n	10016+8n	Scanning time error	



5. 3 INPUT RELAYS (CONTROL SIGNAL) B2801 TO CPU MODULE (Cont'd)

(2) Details of Input Relays

The 16 input relays produce control signals as detailed in Table 5. 8. Numbers after signal names indicate exclusive input relays for counters 1 and 2, respectively.

Table 5. 8 Input Relay Signals

Reference No.		Name	Description
GL20	GL60S		
1001+8n	10001+8n	READY	Shows result of module self-diagnosis. ON for normal, result, OFF for abnormal (e. g., errors in ROM, RAM, WDT and check). It stays OFF for approximately 0. 8 sec for power ON, or module reset.
1002+8n 1009+8n	10002+8n 10009+8n	Preset ACK1 Preset ACK2	Shows that B2801 preset operation has been completed normally. While preset instruction is ON, it stays on (initial setting, current value, coincidence point, count width, stored number, pointer.)
1003+8n 1010+8n	10003+8n 10010+8n	Preset NAK1 Preset NAK2	Indicates that the preset operation in the B2801 is not working correctly. Stays ON while preset instruction is on.
1004+8n 1011+8n	10004+8n 10011+8n	Carry 1 Carry 2	Turns ON for 1 scan when the current counter value changes to 0 after 999, 999 (GL20) or 99, 999, 999 (GL60S).
1005+8n 1012+8n	10005+8n 10012+8n	Borrow 1 Borrow 2	Turns ON for 1 scan when the current counter value gets smaller than 0 and changes to 999, 999 (GL20) or 99, 999, 999 (GL60S).
1006+8n 1013+8n	10006+8n 10013+8n	Coincidence output 1 and 2	Indicates output status of the external coincidence output signal "□EQU". Turns ON when "□EQU" output is ON.
1016+8n	10016+8n	Scanning time error	Turns ON when scanning time of CPU module is too short for the B2801 internal process. OFF is normal (refer to Par. 8.)

(3) Precautions for Input Relays

① “Preset ACK□” and “Preset NAK□” input relays do not respond to preset commands which are not related to counter functions.

Table 5.9 Responses of ACK and NAK

Counter Function \ Preset	Initial Setting	Current Value Preset Command	Coincidence Preset Command	Count Width Preset Command	Stored Number Preset Command	Pointer Command
Comparison Counter	○	○	○	×	×	×
Cyclic Counter	○	○	○	○	×	×
Sampling Counter	○	○	×	×	×	×
Memory Counter	○	○	×	×	○	○

○ : ACK□, NAK□ respond.
 × : ACK□, NAK□ do not respond.

② “Preset ACK□” and “Preset NAK□” input relays stay on while a preset command which satisfies ON conditions is ON. If a successive preset command is given they respond to that command. Fig. 5.1 shows examples of responses. If in the same counter, ACK and NAK do not turn on simultaneously.

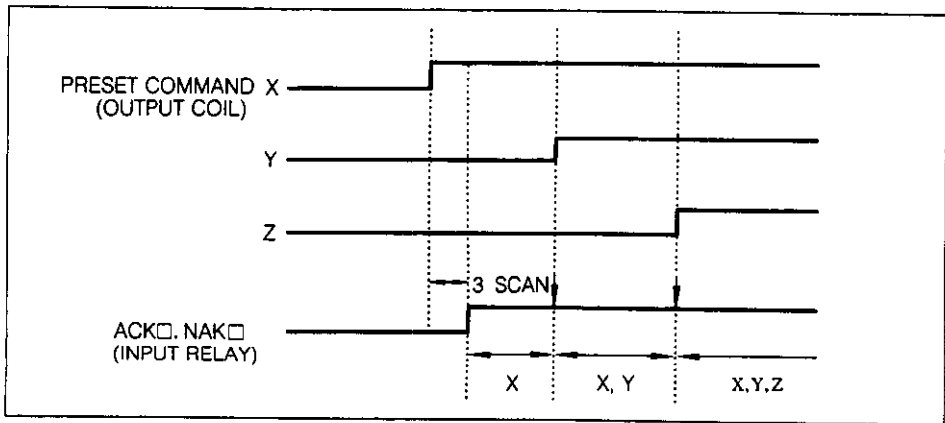
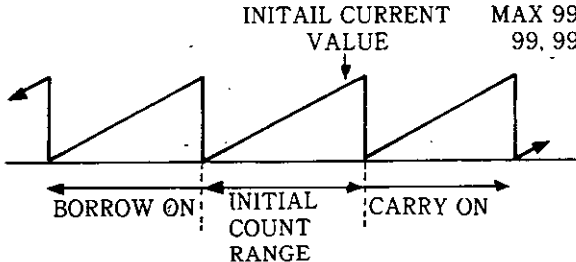


Fig. 5.1 Responses of Preset ACK and NAK

5.3 INPUT RELAYS (CONTROL SIGNAL) B2801 TO CPU MODULE (Cont'd)

③ Input relays "carry□" and "borrow□" change their ON/OFF operation depending on the counter function mode.

Table 5.10 ON/OFF Operations of Carry and Borrow

Input Relay Counter Function	ON/OFF Operation of "Carry" and "Borrow"
<ul style="list-style-type: none"> • Comparison Counter • Cyclic Counter 	Turns on for 1 scan only when carry or borrow is produced again within the same scan it may stay on continuously while monitoring.
<ul style="list-style-type: none"> • Sampling Counter • Memory Counter 	<p>① Carry and borrow observed during monitoring of sampling current value or stored data mean that the initial range of the data has overflowed.</p> <div style="text-align: center;">  </div> <p>Carry or borrow will be reset by going one peak backward.</p> <p>② For other nomitorings they work the same as comparison counter and cyclic counter.</p>

5. 4 OUTPUT REGISTERS (SETTING DATA) CPU MODULE TO B2801

When presetting various setting data to the B2801 from a CPU module four successive output registers are used. The first two registers are exclusively used by counter 1, and the last two by counter 2.

Preset commands which require output registers are; "initial setting", "current value preset command \square ", "coincidence preset command \square ", "count width preset command \square ", "stored number preset command \square ", and "pointer command \square ".

Since the same output registers are used for preset commands care must be taken not to duplicate their timings. One output register will allow 3-digit decimal (GL20), or 4-digit decimal (GL60S). Table 5. 11 shows allocations of output registers.

Table 5. 11 Output Register Allocations (BINARY)

GL20	GL60S	Output Register No.	
4001+n	40001+n	1ST	} Exclusively for Counter 1
4002+n	40002+n	2ND	
4003+n	40003+n	3RD	} Exclusively for Counter 2
4004+n	40004+n	4TH	

n=0, 1, 2...

Reference numbers for output register allocations

5. 4. 1 Initial Settings

Initial settings are used for setting counter functions of the B2801. Initial settings are achieved by setting an initial value to output registers and by output coil command "initial setting".

(1) Initial Setting Items

Table 5. 12 shows initial setting items of the B2801. Counters 1 and 2 can be set in a separate mode.

Table 5. 12 Initial Setting Items

Setting Items	Description												
Pulse Input Mode Setting	Specifies pulse input mode 0 : Pulse with sign 1 : Phases A, B												
Pulse Count Mode Setting	<p>The setting pulse input mode and specifying phases A/B pulse count mode for phases A/B need to be specified. 0 : X1 1 : X2 2 : X4</p> <p>(PULSE COUNT TIMING)</p> <table border="1"> <thead> <tr> <th>MODE</th> <th>ADD COUNT</th> <th>SUBTRACT COUNT</th> </tr> </thead> <tbody> <tr> <td>0</td> <td> </td> <td> </td> </tr> <tr> <td>1</td> <td> </td> <td> </td> </tr> <tr> <td>2</td> <td> </td> <td> </td> </tr> </tbody> </table>	MODE	ADD COUNT	SUBTRACT COUNT	0			1			2		
MODE	ADD COUNT	SUBTRACT COUNT											
0													
1													
2													
Coincidence Output Mode Setting	<p>Valid only when comparison counter function is selected. Specifies a coincidence output mode. 0 : Current value > Coincidence point preset value 1 : Current value = Coincidence point preset value 2 : Current value < Coincidence point preset value</p>												
Counter Function Mode Setting	<p>Specifies functions can be selected for counters 1 and 2 separately. 0 : Comparison counter 1 : Cyclic counter 2 : Sampling counter 3 : Memory counter</p>												

(2) Setting Initial Values to Output Registers

Since initial settings are made to counters 1 and 2 simultaneously, four output registers are required. Table 5. 13 shows methods of setting initial values to output registers.

Figures in frames are default values which are automatically set when turning on power, or resetting modules.

Table 5. 13 Setting of Initial Values to Output Registers
 [GL20 □□□ 3-DIGIT , GL60S □□□□ 4-DIGIT]

Counter 1	Counter 2
<p>1ST</p> <div style="border: 1px solid black; padding: 2px; display: inline-block;">0 0 0 0</div> <ul style="list-style-type: none"> — PULSE INPUT MODE SETTING 0 : PULSE WITH SIGN 1 : PHASES A,B — PHASES A, B PULSE COUNT MODE SETTING 0 : ×1 1 : ×2 2 : ×4 — COINCIDENCE OUTPUT MODE SETTING 0 : CURRENT VALUE > COINCIDENCE POINT PRESET VALUE 1 : CURRENT VALUE = COINCIDENCE POINT PRESET VALUE 2 : CURRENT VALUE < COINCIDENCE POINT PRESET VALUE 	<p>3RD</p> <div style="border: 1px solid black; padding: 2px; display: inline-block;">0 0 0 0</div> <ul style="list-style-type: none"> — PULSE INPUT MODE SETTING 0 : PULSE WITH SIGN 1 : PHASES A, B — PHASES A, B PULSE COUNT MODE SETTING 0 : ×1 1 : ×2 2 : ×3 — COINCIDENCE OUTPUT MODE SETTING 0 : CURRENT VALUE > COINCIDENCE POINT PRESET VALUE 1 : CURRENT VALUE = COINCIDENCE POINT PRESET VALUE 2 : CURRENT VALUE < COINCIDENCE POINT PRESET VALUE
<p>2ND</p> <div style="border: 1px solid black; padding: 2px; display: inline-block;">0 0 0 0</div> <ul style="list-style-type: none"> — COUNTER FUNCTION SETTING 0 : COMPARISON COUNTER 1 : CYCLIC COUNTER 2 : SAMPLING COUNTER 3 : MEMORY COUNTER 	<p>4TH</p> <div style="border: 1px solid black; padding: 2px; display: inline-block;">0 0 0 0</div> <ul style="list-style-type: none"> — COUNTER FUNCTION SETTING 0 : COMPARISON COUNTER 1 : CYCLIC COUNTER 2 : SAMPLING COUNTER 3 : MEMORY COUNTER

- Normal/abnormal check of initial setting values is made for each item. If abnormality is found the particular item retains the previous setting value, while other items are changed to new settings. "Preset NAK 1" and "Preset NAK 2" are turned on.

- All unused digits are regarded as inactive.

5. 4. 2 Data Setting

(1) Setting to Output Registers

Table 5. 14 shows data setting when executing various preset command to output registers.

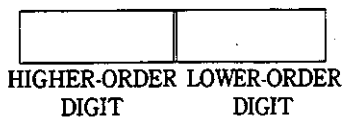
Table 5. 14 Data Setting

Setting Item	Output Register	
	GL20	GL60
<ul style="list-style-type: none"> • Current Value Setting • Coincidence Point Setting • Count Setting 	<p>1ST 2ND EXCLUSIVELY FOR COUNTER 1</p> <p><input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/></p> <p>0 TO 999, 999</p> <p>3RD 4TH EXCLUSIVELY FOR COUNTER 2</p> <p><input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/></p> <p>0 TO 999, 999</p>	<p>1ST 2ND EXCLUSIVELY FOR COUNTER 1</p> <p><input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/></p> <p>0 TO 99, 999, 999</p> <p>3RD 4TH EXCLUSIVELY FOR COUNTER 2</p> <p><input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/></p> <p>0 TO 99, 999, 999</p>
<ul style="list-style-type: none"> • Stored Number Setting • Pointer Width Setting 	<p>1ST 2ND EXCLUSIVELY FOR COUNTER 1</p> <p><input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/></p> <p>NOT USED 0 TO 999</p> <p>3RD 4TH EXCLUSIVELY FOR COUNTER 2</p> <p><input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/></p> <p>NOT USED 0 TO 999</p>	<p>1ST 2ND EXCLUSIVELY FOR COUNTER 1</p> <p><input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/></p> <p>NOT USED 0 TO 999</p> <p>3RD 4TH EXCLUSIVELY FOR COUNTER 2</p> <p><input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/> <input type="text"/></p> <p>NOT USED 0 TO 999</p>

Note :

1. For the stored number and pointer settings, inactive digits are disregarded, although shown on monitor.

2. 1ST(3RD) 2ND(4TH)



5. 5 INPUT REGISTERS (MONITOR DATA) B2801 TO CPU MODULE

When monitoring various data of the B2801 4 consecutive input registers are used. The first two are used exclusively for counter 1, and the last two for counter 2.

Details of monitor data vary depending on monitor code settings (output coil : monitor 0 to 2).

Table 5. 15 Input Register Allocation (BINARY)

GL20	GL60S	Input Register No.	
3001+n	30001+n	1ST	} Exclusively for Counter 1
3002+n	30002+n	2ND	
3003+n	30003+n	3RD	} Exclusively for Counter 2
3004+n	30004+n	4TH	

n=0, 1, 2, ...

Reference numbers for input register allocations

Table 5. 16 Relation of Input Register and Counter

GL20	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center;">1ST 3001+n HIGHER 3- DIGIT</td> <td style="text-align: center;">2ND 3002+n LOWER 3- DIGIT</td> </tr> <tr> <td colspan="2" style="text-align: center;">EXCLUSIVELY FOR COUNTER 1</td> </tr> </table>	1ST 3001+n HIGHER 3- DIGIT	2ND 3002+n LOWER 3- DIGIT	EXCLUSIVELY FOR COUNTER 1		<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center;">3RD 3003+n HIGHER 3- DIGIT</td> <td style="text-align: center;">4TH 3004+n LOWER 3- DIGIT</td> </tr> <tr> <td colspan="2" style="text-align: center;">EXCLUSIVELY FOR COUNTER 2</td> </tr> </table>	3RD 3003+n HIGHER 3- DIGIT	4TH 3004+n LOWER 3- DIGIT	EXCLUSIVELY FOR COUNTER 2	
1ST 3001+n HIGHER 3- DIGIT	2ND 3002+n LOWER 3- DIGIT									
EXCLUSIVELY FOR COUNTER 1										
3RD 3003+n HIGHER 3- DIGIT	4TH 3004+n LOWER 3- DIGIT									
EXCLUSIVELY FOR COUNTER 2										
GL60S	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center;">1ST 30001+n HIGHER 3- DIGIT</td> <td style="text-align: center;">2ND 30002+n LOWER 3- DIGIT</td> </tr> <tr> <td colspan="2" style="text-align: center;">EXCLUSIVELY FOR COUNTER 1</td> </tr> </table>	1ST 30001+n HIGHER 3- DIGIT	2ND 30002+n LOWER 3- DIGIT	EXCLUSIVELY FOR COUNTER 1		<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="text-align: center;">3RD 30003+n HIGHER 3- DIGIT</td> <td style="text-align: center;">4TH 30004+n LOWER 3- DIGIT</td> </tr> <tr> <td colspan="2" style="text-align: center;">EXCLUSIVELY FOR COUNTER 2</td> </tr> </table>	3RD 30003+n HIGHER 3- DIGIT	4TH 30004+n LOWER 3- DIGIT	EXCLUSIVELY FOR COUNTER 2	
1ST 30001+n HIGHER 3- DIGIT	2ND 30002+n LOWER 3- DIGIT									
EXCLUSIVELY FOR COUNTER 1										
3RD 30003+n HIGHER 3- DIGIT	4TH 30004+n LOWER 3- DIGIT									
EXCLUSIVELY FOR COUNTER 2										

5. 5 INPUT REGISTER (MONITOR DATA) B2801 TO CPU MODULE (Cont'd)

Table 5. 17 Input Register Monitor

Description	Input Register	
	GL20	GL60S
<ul style="list-style-type: none"> • Current Counter Value • Current Value Preset • Coincidence Point Preset • Current Sampling Value • Sampling Number • Sampling Stored Data 	1ST 2ND (3RD) (4TH) □□□ □□□ 0 TO 999, 999	1ST 2ND (3RD) (4TH) □□□□ □□□□ 0 TO 99, 999, 999
<ul style="list-style-type: none"> • Stored Preset Value • Pointer Command 	1ST 2ND (3RD) (4TH) □□□ □□□ NOT USED 0 TO 999	1ST 2ND (3RD) (4TH) □□□□ □□□□ NOT USED 0 TO 999
• Initial Setting	Same as the output register of initial setting (refer to Table 5. 9).	

Table 5. 18 Monitor Codes and Monitor Description

Signal Name			Monitor Codes and Monitor Description				
Monitor 0	Monitor 2	Monitor 2	Comparison Counter	Cyclic Counter	Sampling Counter	Memory Counter	
0	0	0	Current counter value	Current counter value	Sampling current value	Stored data	
1	0	0	Current value preset value	Value current preset value	Current value preset value	Current value preset value	
0	1	0	Coincidence point preset value	Coincidence point preset value	Current counter value	Current counter value	
1	1	0	Current counter value	Count width preset value		Sample number	Sample stored number
0	0	1		Current counter value			
1	0	1		Pointer command setting value			
0	1	1		Sample number			
1	1	1	Initial setting	Initial setting	Initial setting	Initial setting	

Note :

1. Sample number - Shows the number of samplings made. It is reset by "initial value setting" or "output disable□" ON.
2. Sample stored number - Shows the number of data stored in the memory counter. It is reset by "initial value setting" or "output disable□" ON.
3. Stored data - Stored data in the memory counter are displayed during pointer command ON and the counter current value is displayed at OFF.

6. EXTERNAL INTERFACE

6.1 B2801 FRONT PANEL ARRANGEMENT

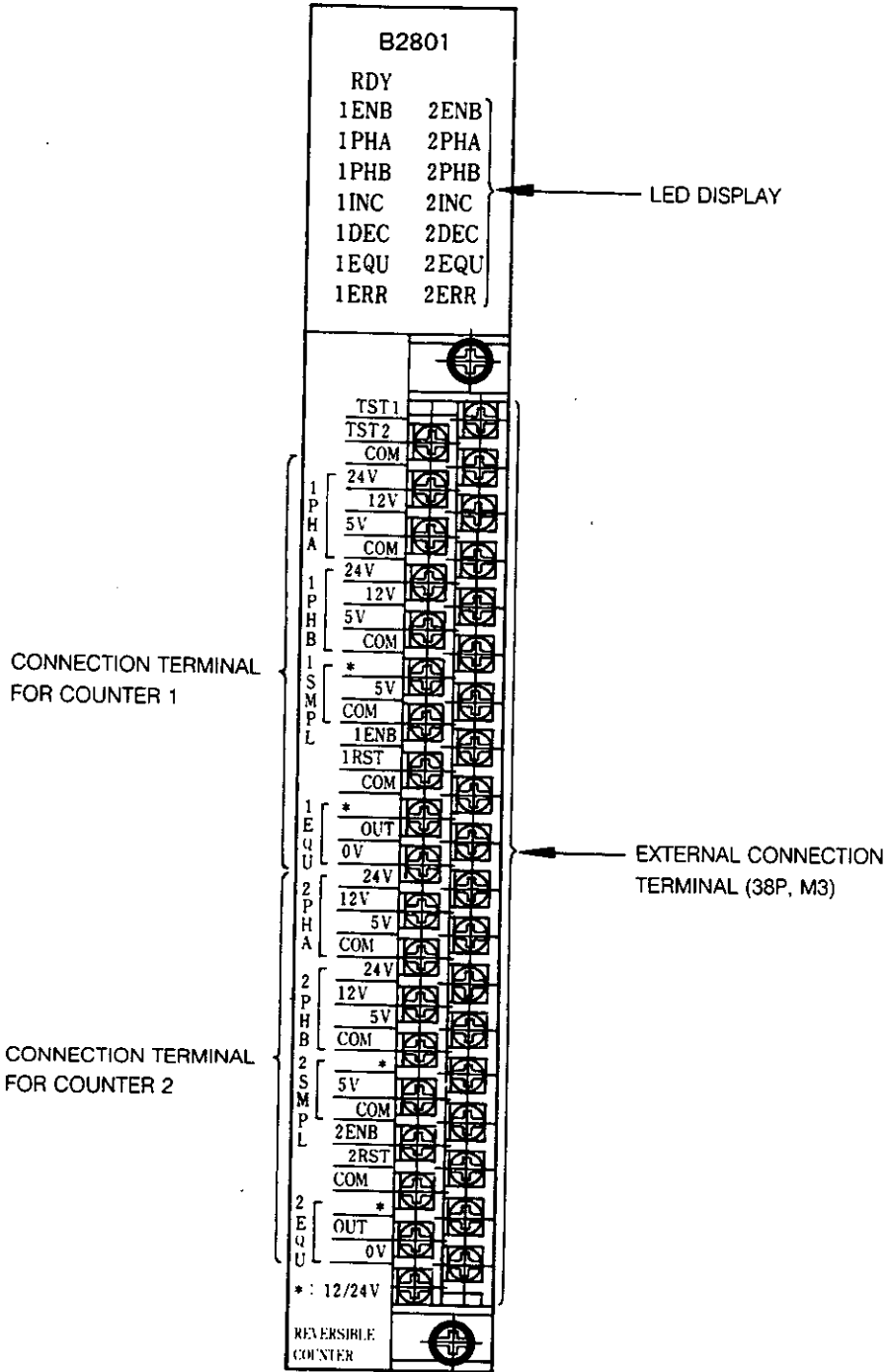


Fig. 6.1 B2801 Front Panel Arrangement

6.2 I/O SIGNAL APPLICATIONS

(1) I/O Signals and Their Description

Table 6.1 I/O Signals and Their Description

Signal Names	Description
TST1 (Add Test Input) TST2 (Subtract Test Input)	Test input terminals for simple count checking. TST1 is used for count test for ADD ition direction, and TST2 for SUBTRACT direction. Turn output coil "count enable□" ON for ADD / SUBTRACT tests. External pulse input count should be stopped in the test modes (refer to Table 6. 3). "□ENB" can be at OFF.
1PHA 2PHA (Phase A : 24, 12, 5V) 1PHB 2PHB (Phase B : 24, 12, 5V)	Pulses fed to phase A and B terminals are counted as current counter values. Select 24V, 12V or 5V terminals depending on the voltage level of signals. Either pulse system for phase A and B, or sign with pulse system can be selected for the input system. For the pulse with sign system, feed the sign to phase B and the pulse to phase A. For the pulse system for phases A and B a pulse count mode of X1, X2, and X4 can be selected. The sign with pulse system is good for an X1 count only. These selections are made by initial settings. (Refer to Table 6. 4.)
1ENB 2ENB (External Count Enable Input)	Input signal to enable the counter to count. Count can be made when "□ENB" is ON and at the same time output coil "count enable□" is ON.
1RST 2RST (External Reset Input)	While "□RST" is ON counter current value is reset. Pulse count is stopped. It forms an OR condition with the output coil "current value reset□".
1EQU 2EQU (External Coincidence Output)	With the comparison counter and cyclic counter functions coincidence signal is output based on the result of a comparison between current counter value and coincidence point current value. With the memory counter function, a specified number of memories are coincidence output to the sampling preset. When output coil "forced coincidence output□" is ON, external coincidence output becomes ON. It becomes effective when output coil "output disable□" is OFF. When a CPU module is stopped by PP (programming panel), the external coincidence output becomes OFF.

Note : Except for TST terminals, 1 and 2 after signal names indicate that they are external I/O signals exclusively for counters 1 and 2, respectively.

(2) I/O Signals and Their Electrical Characteristics

Table 6. 2 I/O Signals and Their Electrical Specifications

Signal Name	Terminal No.		Internal Circuit	Electrical Specification		
	Count 1	Count 2			Operation Voltage	Operation Current
TST1 (ADD Test Input)	1				10.2 to 26.4V	4 to 12mA
TST2 (SUBTRACT Test Input)	2				3V	0.5mA
COM	3				ON Response Time : 120ms or less OFF Response Time : 120ms or less	
<input type="checkbox"/> P <input type="checkbox"/> H <input type="checkbox"/> A	24V (Phase A Pulse Input)	4 21			20.4 to 26.4V	7 to 11mA
	12V (Phase A Pulse Input)	5 22			3V	0.3mA
	5V (Phase A Pulse Input)	6 23			10.2 to 13.2V	7 to 11mA
	COM	7 24			2V	0.3mA
<input type="checkbox"/> P <input type="checkbox"/> H <input type="checkbox"/> B	24V (External Sampling Input)	8 25			4.5 to 5.5V	7 to 11mA
	12V (External Sampling Input)	9 26			1V	0.3mA
	5V	10 27			ON Response Time : 1ms or less OFF Response Time : 1ms or less	
	COM	11 28				
<input type="checkbox"/> P <input type="checkbox"/> H <input type="checkbox"/> B	12/24V	12 29			10.2 to 26.4V	4 to 11mA
	5V	13 30			3V	0.5mA
	COM	14 31			4.5 to 5.5V	6 to 7.5mA
					1V	0.5mA
				ON Response Time : 1ms or less OFF Response Time : 1ms or less		
<input type="checkbox"/> ENB (External Count Enable Input)	15	32			10.2 to 26.4V	4 to 12mA
<input type="checkbox"/> RST (External Reset Input)	16	33			3V	0.5mA
COM	17	34			(OFF ON Response Time) External Count Enable : 1ms or less External Reset : 6ms or less (ON OFF Response Time) External Count Enable : 2ms or less External Reset : 4ms or less	
<input type="checkbox"/> P <input type="checkbox"/> H <input type="checkbox"/> B	12/24 (Power Supply Input)	18 35			10.2 to 26.4V	4mA or less
	OUT (External Coincidence Output)	19 36			29V	250mA
	OV	20 37			1.5V or less	5ms or less
					5ms or less	

6. 2 I/O SIGNAL APPLICATIONS (Cont'd)

(3) Test Input Count Timing

Table 6. 3 TEST1 and TEST2 Count Timing

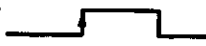

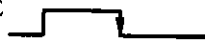





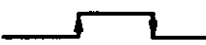

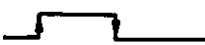



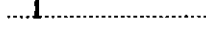
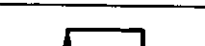

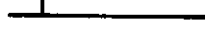
	ADD	SUBTRACT
1 If ON time is less than one sec it becomes one pulse ADD / SUBTRACT.	<p>TEST 1 OFF</p> <p>ON</p> <p>TEST 2 OFF</p> <p>$t < 1s$</p> <p>No+1</p>	<p>TEST 1 OFF</p> <p>ON</p> <p>TEST 2 OFF</p> <p>$t < 1s$</p> <p>No-1</p>
2 If ON time is more than one sec it becomes ten pulse ADD / SUBTRACT	<p>TEST 1 OFF</p> <p>ON</p> <p>TEST 2 OFF</p> <p>1s 1s 1s</p> <p>No+10 No+20 No+20</p>	<p>TEST 1 OFF</p> <p>ON</p> <p>TEST 2</p> <p>1s 1s 1s</p> <p>No-10 No-20 No-20</p>
3 If TEST1 and TEST2 are simultaneously ON count is stopped.	<p>TEST 1</p> <p>TEST 2</p> <p>No+0</p>	

Note :

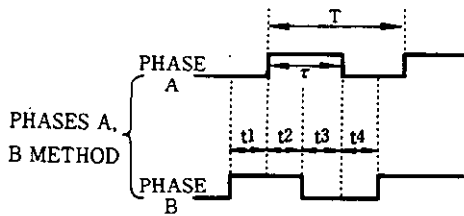
1. Output coil "count enable" should be ON for test input mode.
2. "No" shows initial values.

(4) Pulse Count Timing

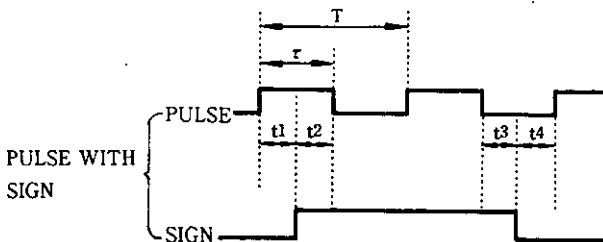
Table. 6. 4 External Input Pulse Count Timing

Pulse Input Mode	Pulse Count Mode	ADD	SUBTRACTION
Phases A and B	×1	PHASE A  PHASE B 	PHASE A  PHASE B 
	×2	PHASE A  PHASE B 	PHASE A  PHASE B 
	×4	PHASE A  PHASE B 	PHASE A  PHASE B 
Pulse With Sign	×1	PHASE A  (PULSE) PHASE B  (SIGN) 	PHASE A  (PULSE) PHASE B  (SIGN) 

Pulse Waveform



FREQUENCY: $T \geq 20 \mu s$
 DUTY RATIO: $\frac{\tau}{T} \times 100 = 50 \pm 10\%$
 $t1, t2, t3, t4, \geq 4 \mu s$



FREQUENCY: $T \geq 20 \mu s$
 DUTY RATIO: $\frac{\tau}{T} \times 100 \geq 40\%$
 $t1, t2, t3, t4, \geq 4 \mu s$

6.3 PRECAUTIONS FOR I/O TERMINAL CONNECTION AND WIRING

6.3.1 I/O Terminal Connection

(1) TST1, and TST2 Terminal Connection

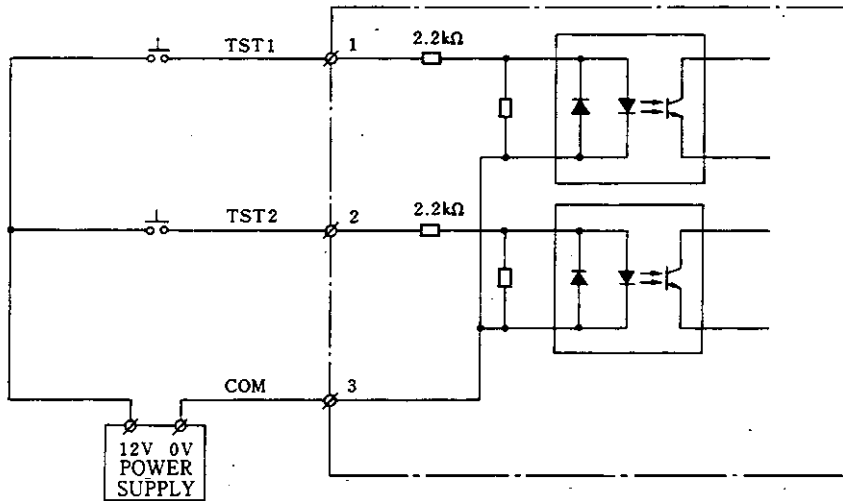


Fig. 6.2 TST1 and TST2 Connection Example

(2) Phases A/B Pulse Input Terminal Connection

① When the pulse generator is open collector output (12V)

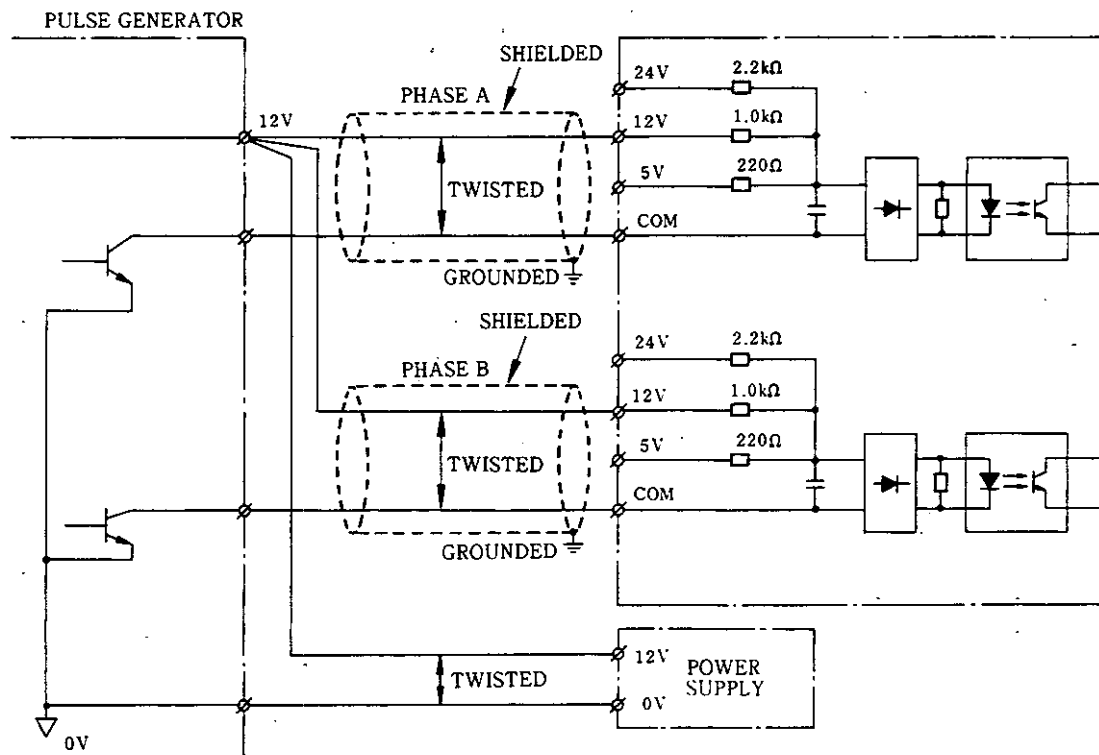


Fig. 6.3 When the Pulse Generator is Open Collector Output (12V)

① When the pulse generator is source voltage output (5V)

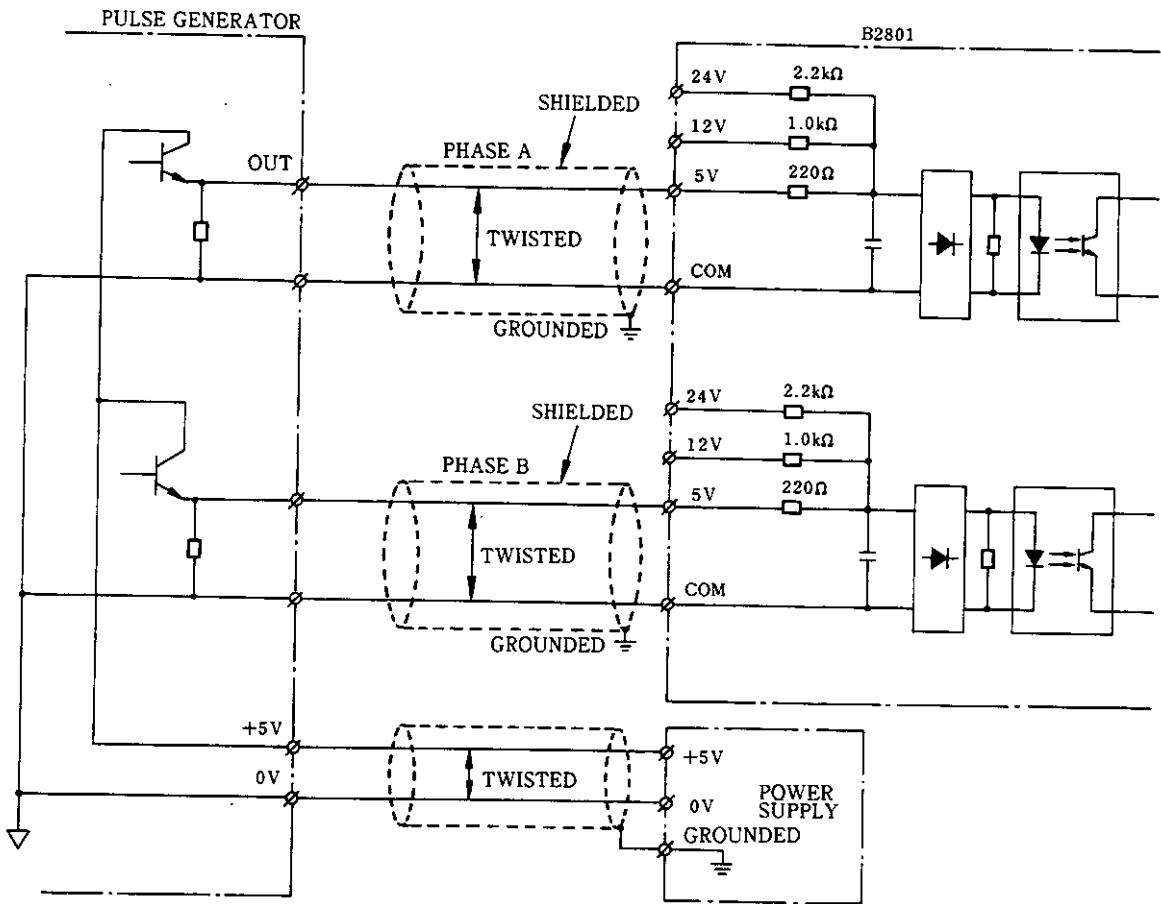


Fig. 6. 4 When the Pulse Generator is Source Voltage Output (5V)

6.3.1 I/O Terminal Connection (Cont'd)

(3) External Sampling Input Terminal Connection (Open Corrector 5V)

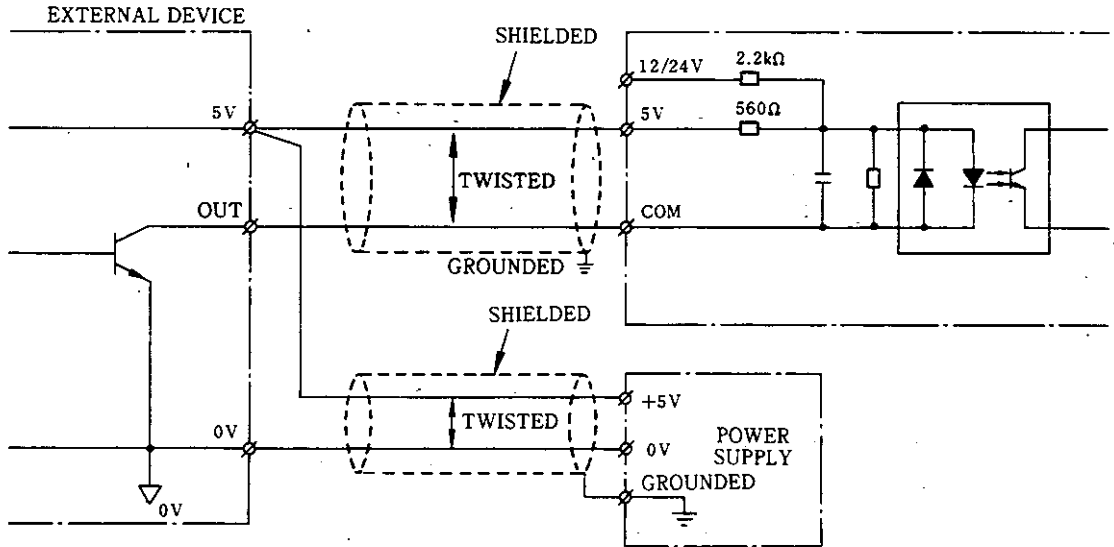


Fig. 6.5 External Sampling Input Terminal Connection Example

(4) ENB, RST Terminal Connection (Open Corrector 12/24V)

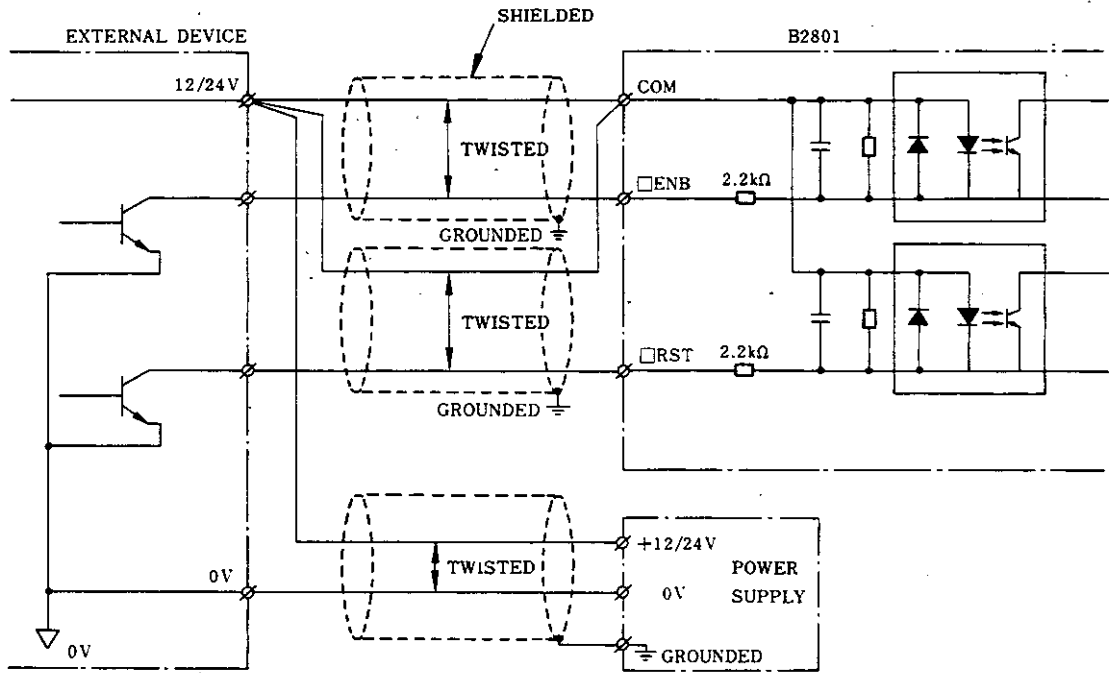


Fig. 6.6 ENB and RST Terminal Connection Example

(5) External Coincidence Output Connection Example

- Connection example for inductive load

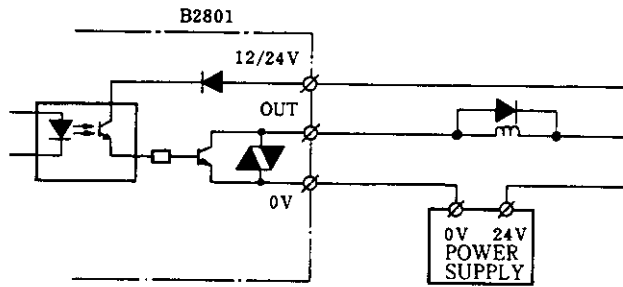


Fig. 6. 7 Connection Example for Inductive Load

6. 3. 2 Precautions about Wiring

- (1) Make sure to use shielded twisted pair wires for signal lines.
- (2) 30m (100 feet) at 50 kpps is a reference wire length. The shorter the better.
- (3) Ground the shield of wire at a single point.
- (4) To avoid malfunctions by noise take the following measures.
 - Insert surge killers in coils for relays, contacts and solenoids.
 - Provide separation of at least 30cm (one foot) between power lines (AC line, I/O lines) and DC signal lines. Never bundle them together or route them in the same duct.
- (5) External Power Supply.
 - For external power supply use general DC stabilized power supply.
 - Provide line filter at the DC stabilized power supply AC input side, so that primary and secondary sides of line filter and DC output side are not run in the same duct.

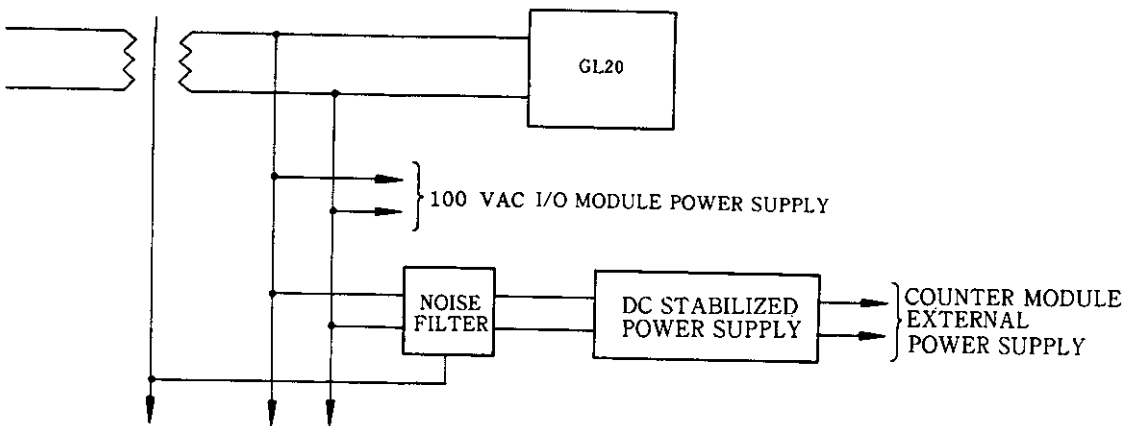


Fig. 6. 8 Counter Module External Power Supply

6. 4 INDICATORS

Table 6. 5 shows description of LED indicators.

Table 6. 5 LED Indicator

Name	Description	
RDY	Indicates result of module self-diagnosis (linked with input relay "READY").	
For Counter 1	1ENB	Lights under the count enable state (when external input "1ENB" is ON and output coil "count enable 2" is ON.)
	1PHA	Lights when a signal is fed to phase A.
	1PHB	Lights when a signal is fed to phase B.
	1INC	Lights during ADD count.
	1DEC	Lights during SUBTRACT count.
	1EQU	Lights during external coincidence output signal "1EQU" is being output.
	1ERR	Lights when preset error or scanning time error occurs.
For Counter 2	2ENB	Lights under the count enable state (when external input "2ENB" is ON and output coil "count enable 2" is ON.)
	2PHA	Lights when a signal is fed to phase A.
	2PHB	Lights when a signal is fed to phase B.
	2INC	Lights during ADD count.
	2DEC	Lights during SUBTRACT count.
	2EQU	Lights when external coincidence output signal "2EQU" is being output.
	2ERR	Lights when preset error or scanning time error occurs.

6. 5 SWITCH SETTING

The following shows select switches of 6-digit mode (with GL20)/8-digit mode (with GL60S).

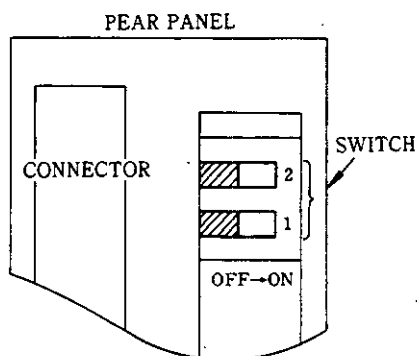


Table 6. 6 Switch Setting

(SW-)	OFF	ON
1	6- digit mode (GL20)	8- digit mode (GL60S)
2	Not used.	

Both SW-1 and -2 are off when delivery.

Fig. 6. 9 Switch Setting Position

7. TEST RUN

7.1 PRECAUTIONS BEFORE TEST RUN

Before turning the power on check wiring and connections.

- (1) Are the switch settings correct for the CPU module ?
- (2) Is the voltage level of the B2801 input terminals correctly set ?
Wrong wiring may damage the units.
- (3) Is wiring for each terminal correct ?

7.2 POWER ON

- (1) After switch settings of the B2801 and wiring are checked correct, turn the power switch on.
 RDY lights when self-diagnosis of the module is completed without any trouble.
- (2) Operate the pulse generator.
 PHA and PHB blinks for phase A, B inputs. PHA blinks for pulse with sign input.
- (3) Verify whether directions of ADD/SUBTRACT by the pulse generator and that of B2801 coincide by INC and DEC.
 - Set the counter to count enable. ENB should light.
 - Operate the pulse generator. INC should light for ADD direction and DEC should light for SUBTRACT direction.

8. ERRORS AND CORRECTIVE MEASURES

8.1 SELF DIAGNOSIS OF B2801

(1) Self diagnosis of the B2801 include the following :

- ① During power up
 - ROM total sum check
 - RAM check

- ② During operation
 - ROM total sum check
 - WDT check
 - Various setting errors
 - Monitoring of CPU module scanning time
 - RUN/STOP status check of CPU module

(2) Corrective Measures to take against errors

Table 8. 1 shows error symptoms and required corrective measures.

Table 8. 1 Error Displays and corrective Measures

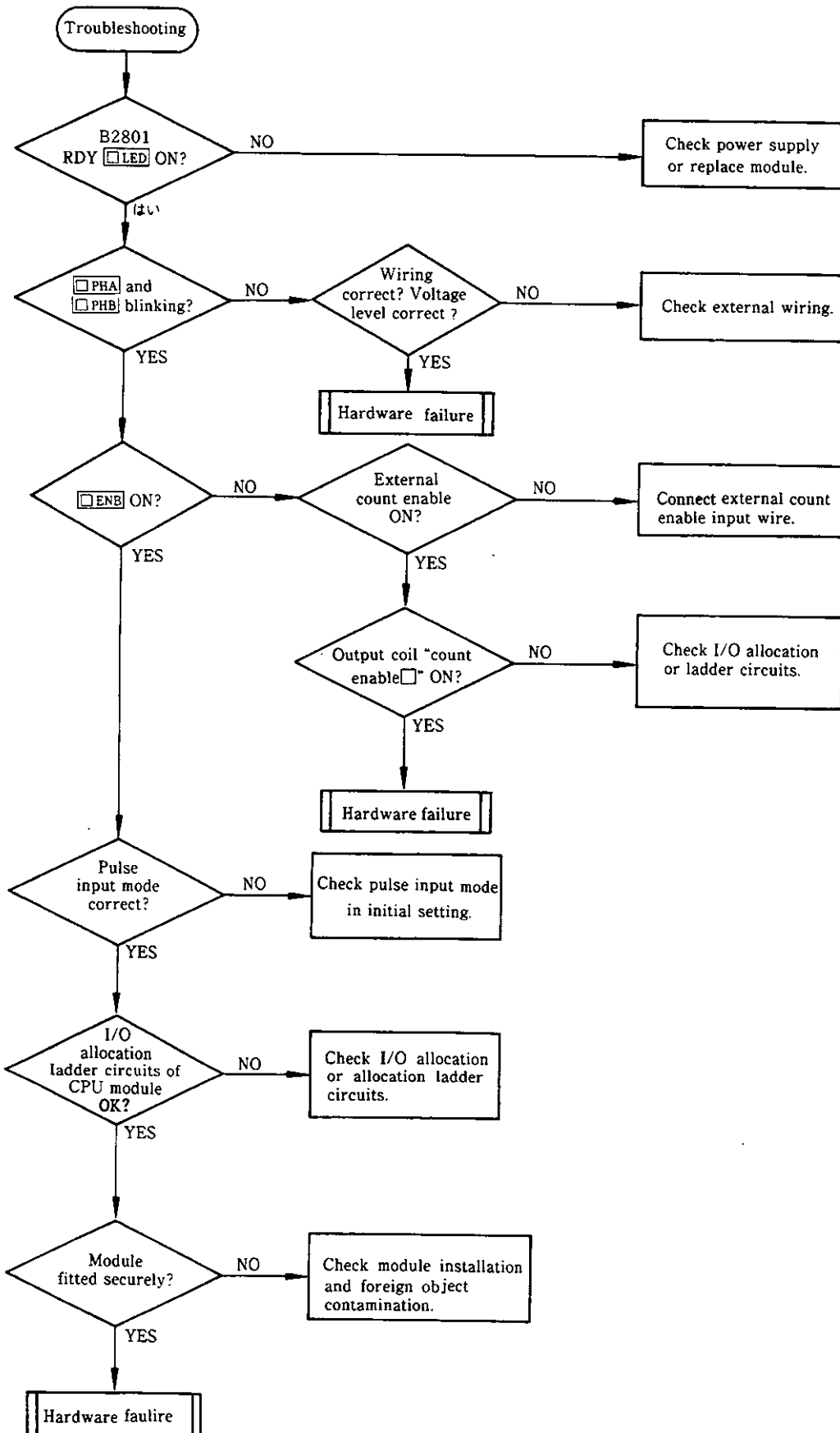
Error	Input Relay		LED Indicator		Corrective Measures
	READY	Scanning Time Error	RDY	<input type="checkbox"/> ERR	
ROM, RAM Check Error WDT Error	OFF	OFF	OFF	ON or OFF	Reset the module or turn the internal power supply off and then on again. If the same errors are found, replace the B2801.
Setting Error	ON	OFF	ON	ON	Replace correct settings.
Service Scan Time of CPU Module is too Short.	ON	ON	ON	ON	This error occurs when very few if any, ladder circuits are stored in the CPU module. Add more ladder circuits or dummy allocations.

When a CPU module is stopped by the programming panel, the external coincidence output becomes OFF, but count continues. Therefore, when the CPU module is started again current counter value may change, resulting in change of state in the external coincidence output.

8.2 SYSTEM ERROR SYMPTOMS AND THEIR REMEDIES

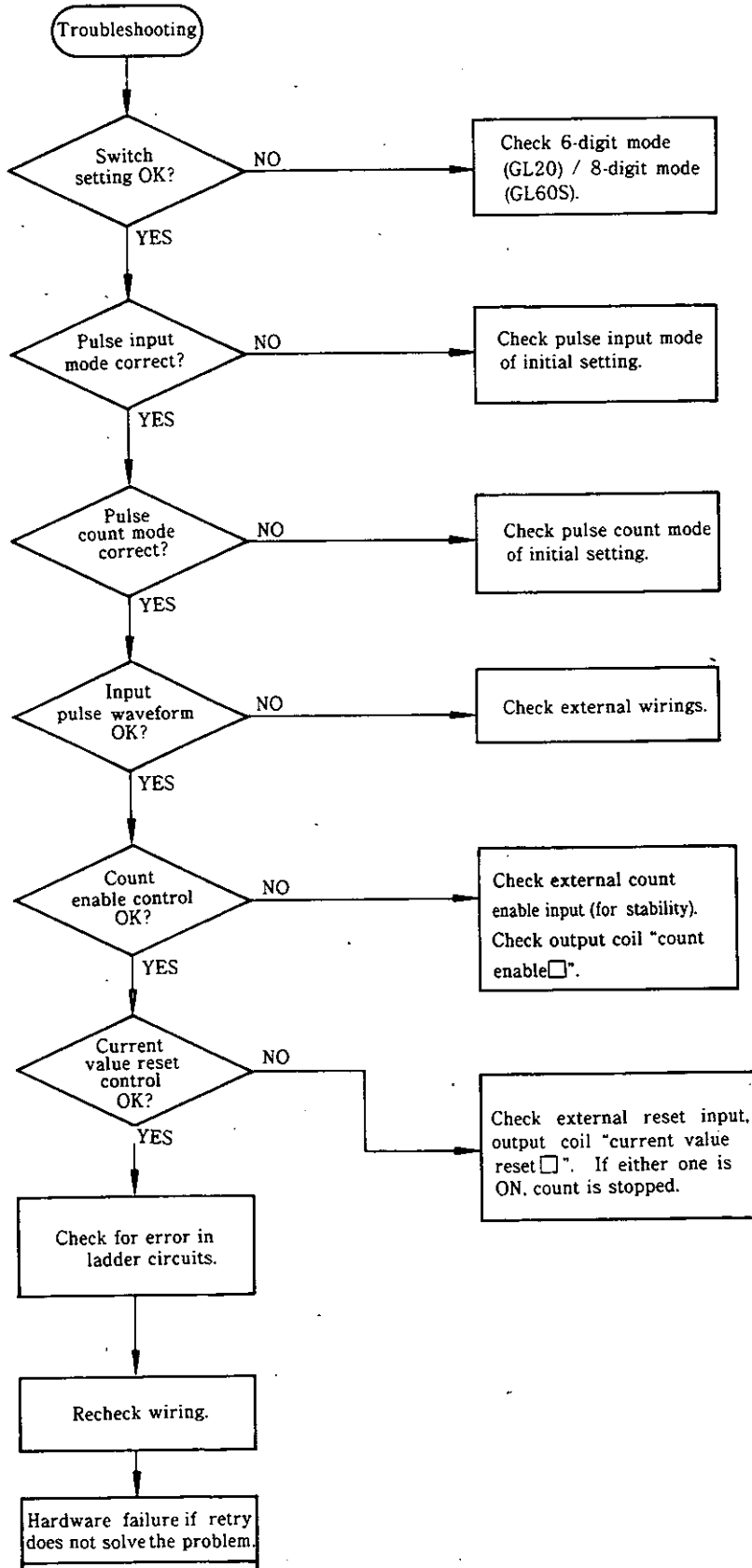
When encountering a problem, first check and verify whether the problem is due to operational error and due to equipment failure.

(1) No Count Function on B2801.

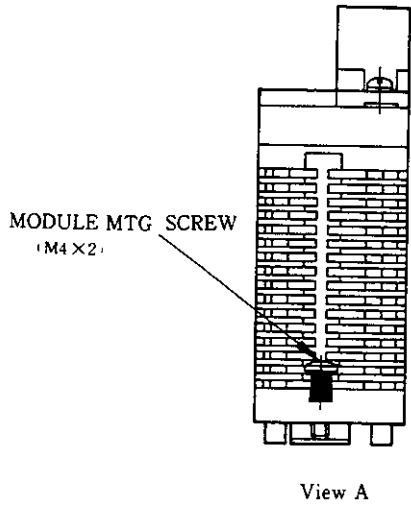
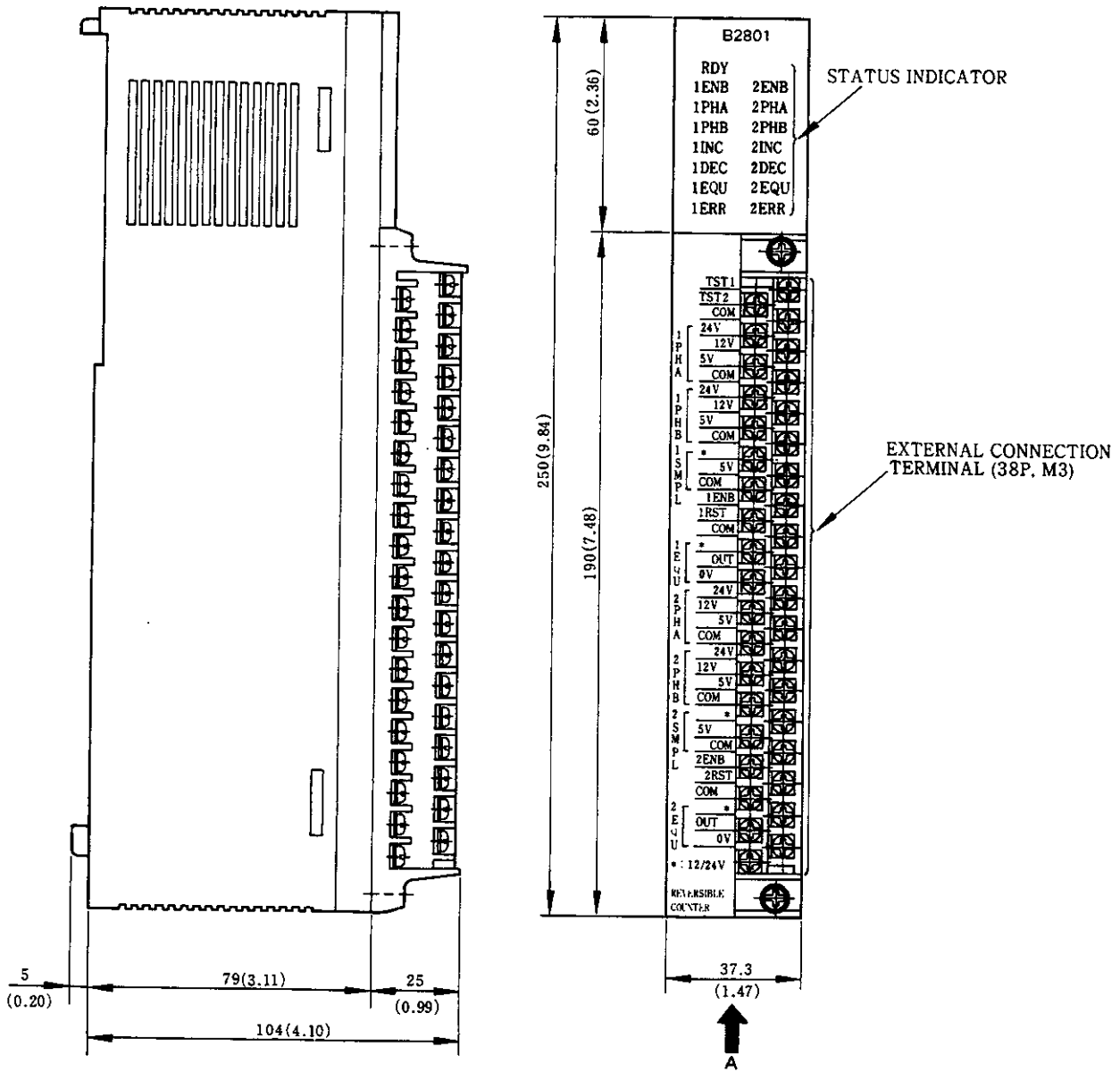


8. 2 SYSTEM ERROR SYMPTOMS AND THEIR REMEDIES (Cont'd)

(2) B2801 Count Function But Incorrect Values



9 DIMENSIONS in mm (inches)



APPENDIX 1 COUNTER OPERATION APPLICATION EXAMPLE

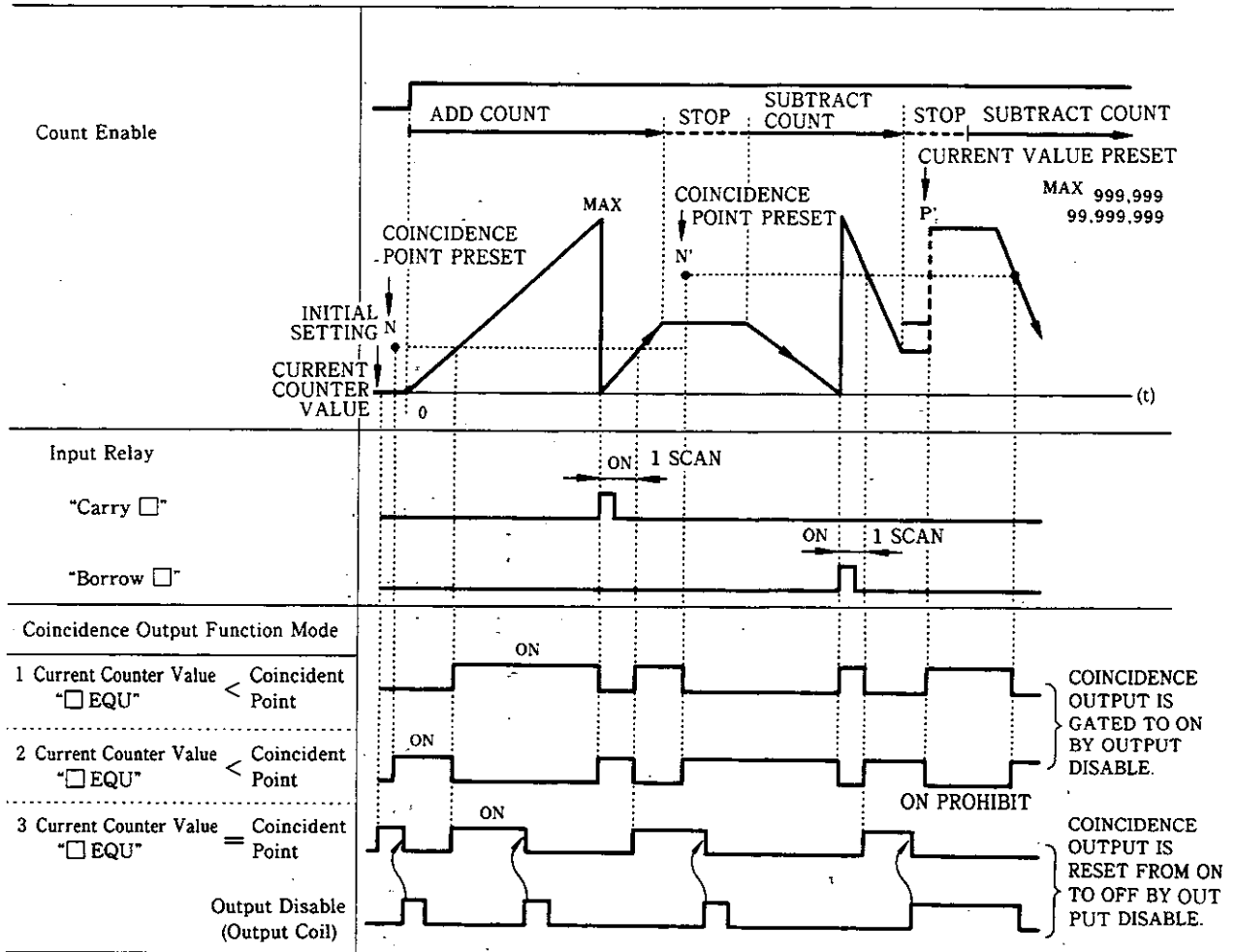


Fig. A1. 1 Comparison Counter Operation (Application Example)

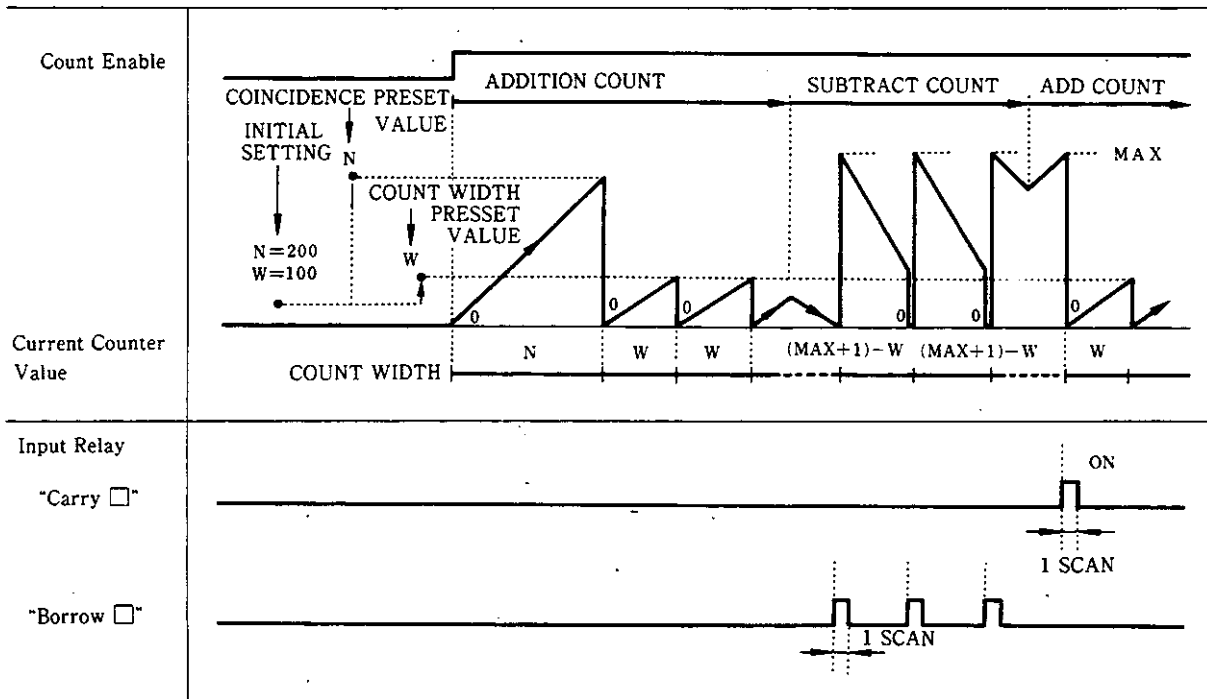



Fig. A1. 2 Cyclic Counter Operation (Application Example)

APPENDIX 2 INTERNAL INTERFACE SIGNAL LIST

Table A2.1 Output Coil List

GL20	GL60S	Signal Name
0001+8n	00001+8n	Module reset
0002+8n	00002+8n	Initial setting
0003+8n	00003+8n	Current value reset 1
0004+8n	00004+8n	Count enable 1
0005+8n	00005+8n	Output disable 1
0006+8n	00006+8n	Current value preset command 1
0007+8n	00007+8n	Coincidence point preset command 1
0008+8n	00008+8n	Count width preset command 1
0009+8n	00009+8n	Stored number preset command 1
0010+8n	00010+8n	Pointer command
0011+8n	00011+8n	Force coincidence output
0012+8n	00012+8n	Monitor 0
0013+8n	00013+8n	Monitor 1
0014+8n	00014+8n	Monitor 2
0015+8n	00015+8n	Current value reset 2
0016+8n	00016+8n	Current enable 2
0017+8n	00017+8n	Output disable 2
0018+8n	00018+8n	Current value preset command 2
0019+8n	00019+8n	Coincidence point preset command 2
0020+8n	00020+8n	Count width preset command 2
0021+8n	00021+8n	Stored number preset command 2
0022+8n	00022+8n	Pointer command 2
0023+8n	00023+8n	Forced coincidence output 2
0024+8n	00024+8n	For future use




 n=0, 1, 2 ...

 Reference numbers for output coil allocations

Table A2.2 Input Relay List

GL20	GL60S	Signal Name
1001+8n	10001+8n	READY
1002+8n	10002+8n	Preset ACK1
1003+8n	10003+8n	Preset NAK1
1004+8n	10004+8n	Carry 1
1005+8n	10005+8n	Borrow 1
1006+8n	10006+8n	Coincidence output 1
1007+8n	10007+8n	Not used
1008+8n	10008+8n	Not used
1009+8n	10009+8n	Preset ACK2
1010+8n	10010+8n	Preset NAK2
1011+8n	10011+8n	Carry 2
1012+8n	10012+8n	Borrow 2
1013+8n	10013+8n	Coincidence output 2
1014+8n	10014+8n	Not used
1015+8n	10015+8n	Not used
1016+8n	10016+8n	Scanning time error



 n=0, 1, 2 ...

 Reference numbers for input relay allocations

APPENDIX 2 INTERNAL INTERFACE SIGNAL LIST (Cont'd)

Table A2. 3 Output Register Allocations

GL20	GL60S	Output Register No.	
4001+n	40001+n	1ST	} Exclusively for Counter 1
4002+n	40002+n	2ND	
4003+n	40003+n	3RD	} Exclusively for Counter 2
4004+n	40004+n	4TH	

n=0, 1, 2, ...

Reference numbers for output registers allocations

Table A2. 4 Initial Values Setting to Output Registers
[GL20 □□□ (3-DIGIT) GL60S □□□□ (4-DIGIT)]

For Counter 1	For Counter 2
<p>3RD 0101010</p> <p>PULSE INPUT MODE SETTING 0: PULSE WITH SIGN 1: PHASES A,B</p> <p>PHASES A, B PULSE COUNT MODE SETTING 0: ×1 1: ×2 2: ×4</p> <p>COINCIDENCE OUTPUT MODE SETTING 0: CURRENT VALUE > COINCIDENCE POINT PRESET VALUE 1: CURRENT VALUE = COINCIDENCE POINT PRESET VALUE 2: CURRENT VALUE < COINCIDENCE POINT PRESET VALUE</p>	<p>1ST 0101010</p> <p>PULSE INPUT MODE SETTING 0: PULSE WITH SIGN 1: PHASES A, B</p> <p>PHASES A, B PULSE COUNT MODE SETTING 0: ×1 1: ×2 2: ×3</p> <p>COINCIDENCE OUTPUT MODE SETTING 0: CURRENT VALUE > COINCIDENCE POINT PRESET VALUE 1: CURRENT VALUE = COINCIDENCE POINT PRESET VALUE 2: CURRENT VALUE < COINCIDENCE POINT PRESET VALUE</p>
<p>2ND 0101010</p> <p>COUNTER FUNCTION SETTING 0: COMPARISON COUNTER 1: CYCLIC COUNTER 2: SAMPLING COUNTER 3: MEMORY COUNTER</p>	<p>4TH 0101010</p> <p>COUNTER FUNCTION SETTING 0: COMPARISON COUNTER 1: CYCLIC COUNTER 2: SAMPLING COUNTER 3: MEMORY COUNTER</p>

Note:

1. For initial settings normal/abnormal check is made for each item. If abnormality is found in an item, that particular item retains an old setting value, while values of other items are updated. "Preset NAK1" and "preset NAK2" come ON.
2. Digits which are not used are all processed as inactive.

Table A2. 5 Input Register Allocations

GL20	GL60S	Input Register No.	
$3001+n$	$30001+n$	1ST	} Exclusively for Counter 1
$3002+n$	$30002+n$	2ND	
$3003+n$	$30003+n$	3RD	} Exclusively for Counter 2
$3004+n$	$30004+n$	4TH	

$n=0, 1, 2, \dots$

Reference numbers for input register allocations

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